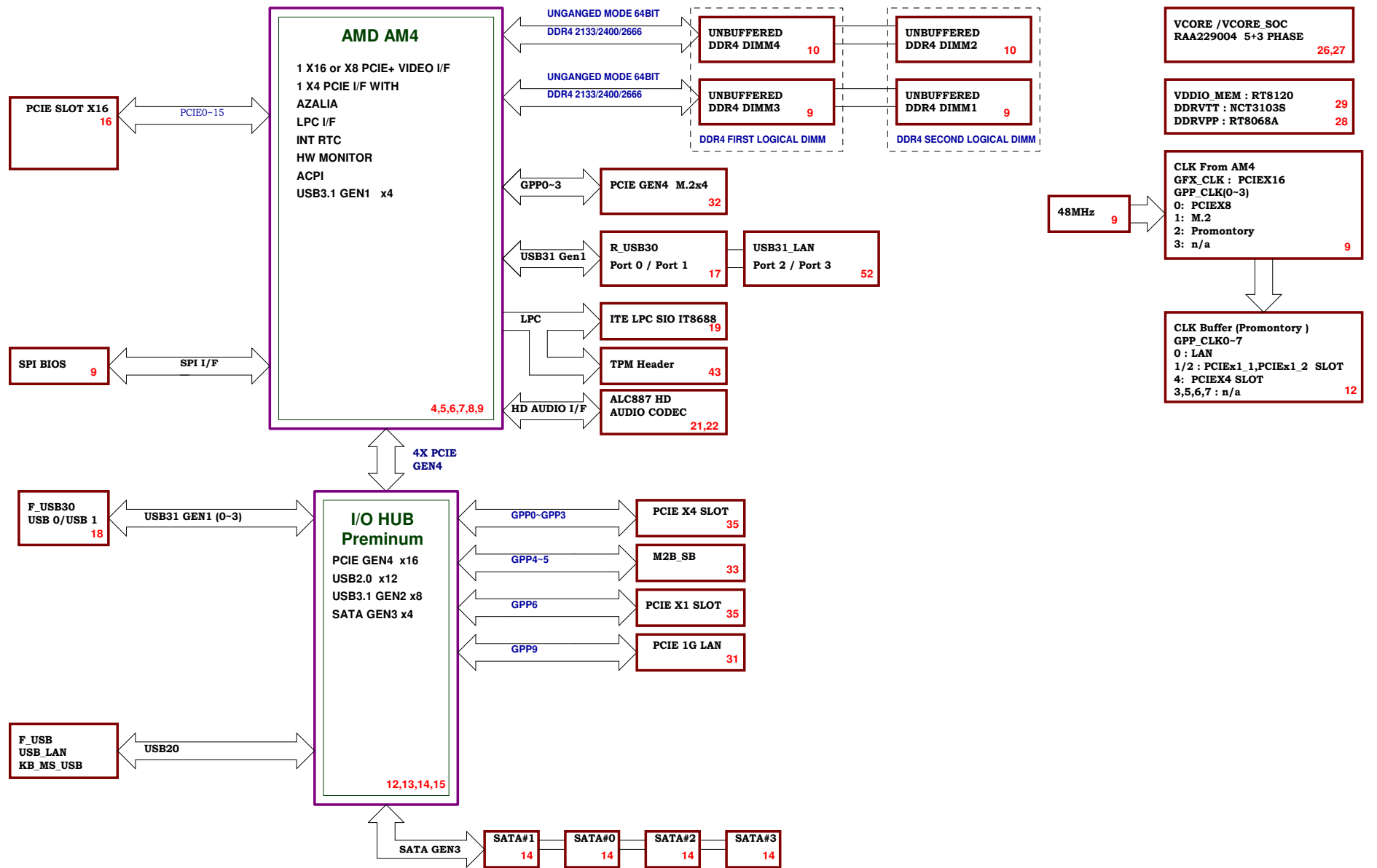


# B550M AORUS ELITE

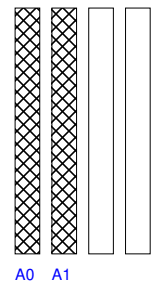
PAGE	TITLE	Revision : 1.01
01	COVER SHEET	
02	BOM & PCB MODIFY HISTORY	
03	BLOCK DIAGRAM	
04	CPU DDR4 MEMORY	
05	CPU CONTROL	
06	CPU GFX, GPP, SB, GND	
07	CPU ACPI/GPIO/USB/AUDIO	
08	CPU POWER & GND	
09	CPU CLK/SPI/USB	
10	DDR4 CHANNEL A	
11	DDR4 CHANNEL B	
12	PM CLK/GPIO/FAN	
13	PM USB	
14	PM UMI/GPP/SATA	
15	PM POWER & GND	
16	PCI EXPRESS x16	
17	PCI EXPRESS x4 / x1	
18	IT8688	
19	FAN. HWM, TPM	
20	PWM RAA229004	
21	VCORE MOS1	
22	VCORE MOS2	
29	POWER SEQ, A_VDDP	
30	DDR POWER , 5VDUAL	
31	VPPMEM, OC DAC	

[illegible]

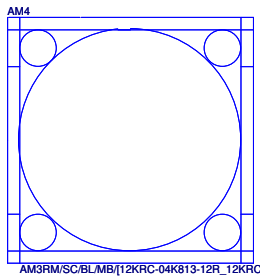




MEM CHA



- [10] MODT\_A[0..3] <=> MODT\_A[0..3]
- [10] MDA[0..63] <=> MDA[0..63]
- [10] MAAA[0..17] <=> MAAA[0..17]
- [10] DQSA[0..8] <=> DQSA[0..8]
- [10] -DQSA[0..8] <=> -DQSA[0..8]



2020.02.17  
12KRC-04K813-12R/14R  
抽芽式

- [11] MODT\_B[0..3] <=> MODT\_B[0..3]
- [11] MDB[0..63] <=> MDB[0..63]
- [11] MAAB[0..17] <=> MAAB[0..17]
- [11] DQSB[0..8] <=> DQSB[0..8]
- [11] -DQSB[0..8] <=> -DQSB[0..8]

**GIGABYTE**™

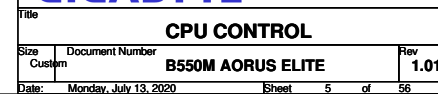
Title: **APU DDR4**

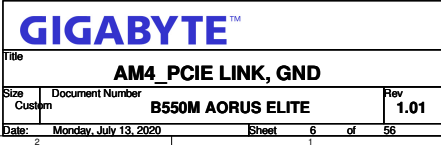
Size: Custom Document Number: **B550M AORUS ELITE** Rev: **1.01**

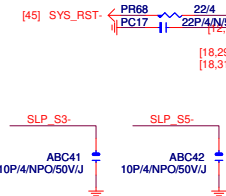
Date: Monday, July 13, 2020 Sheet: 4 of 56

A0 A1

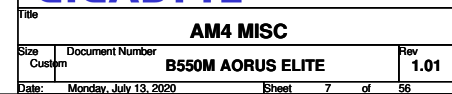
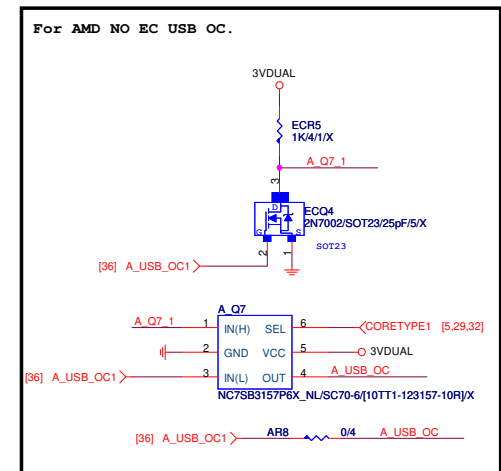
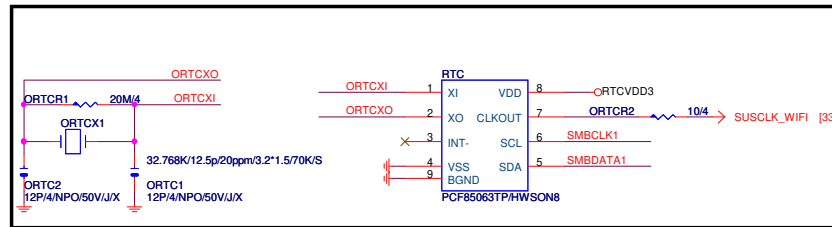
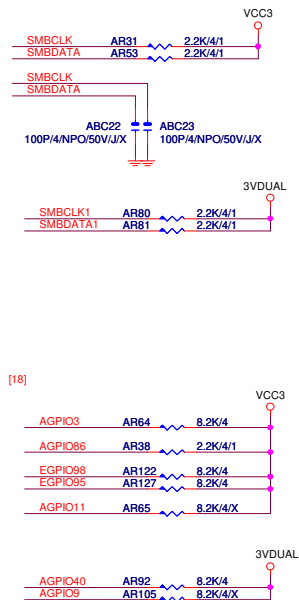
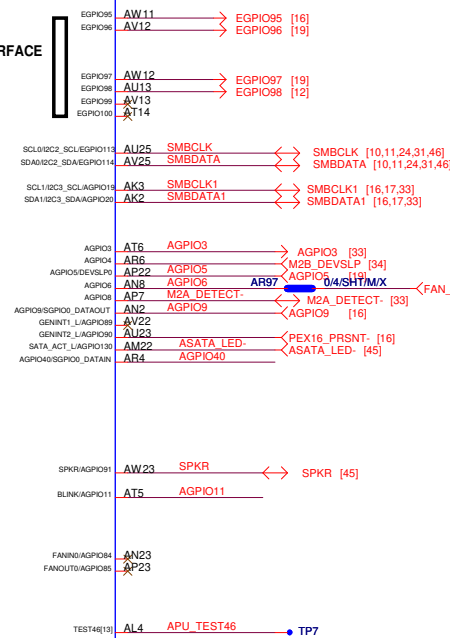
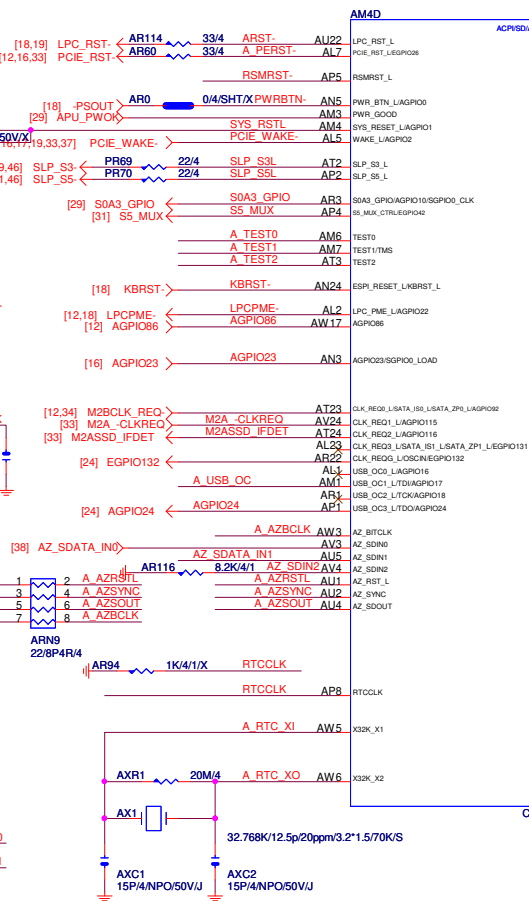
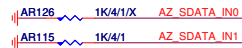
B0 B1







TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.



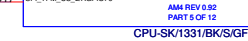






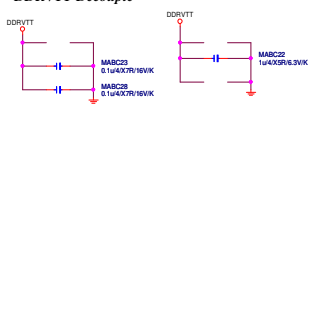
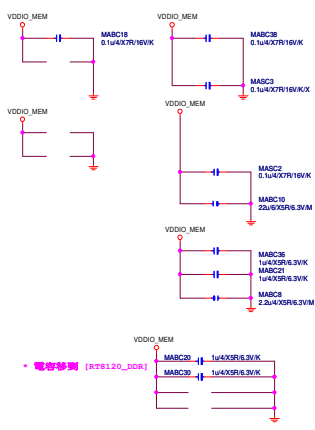
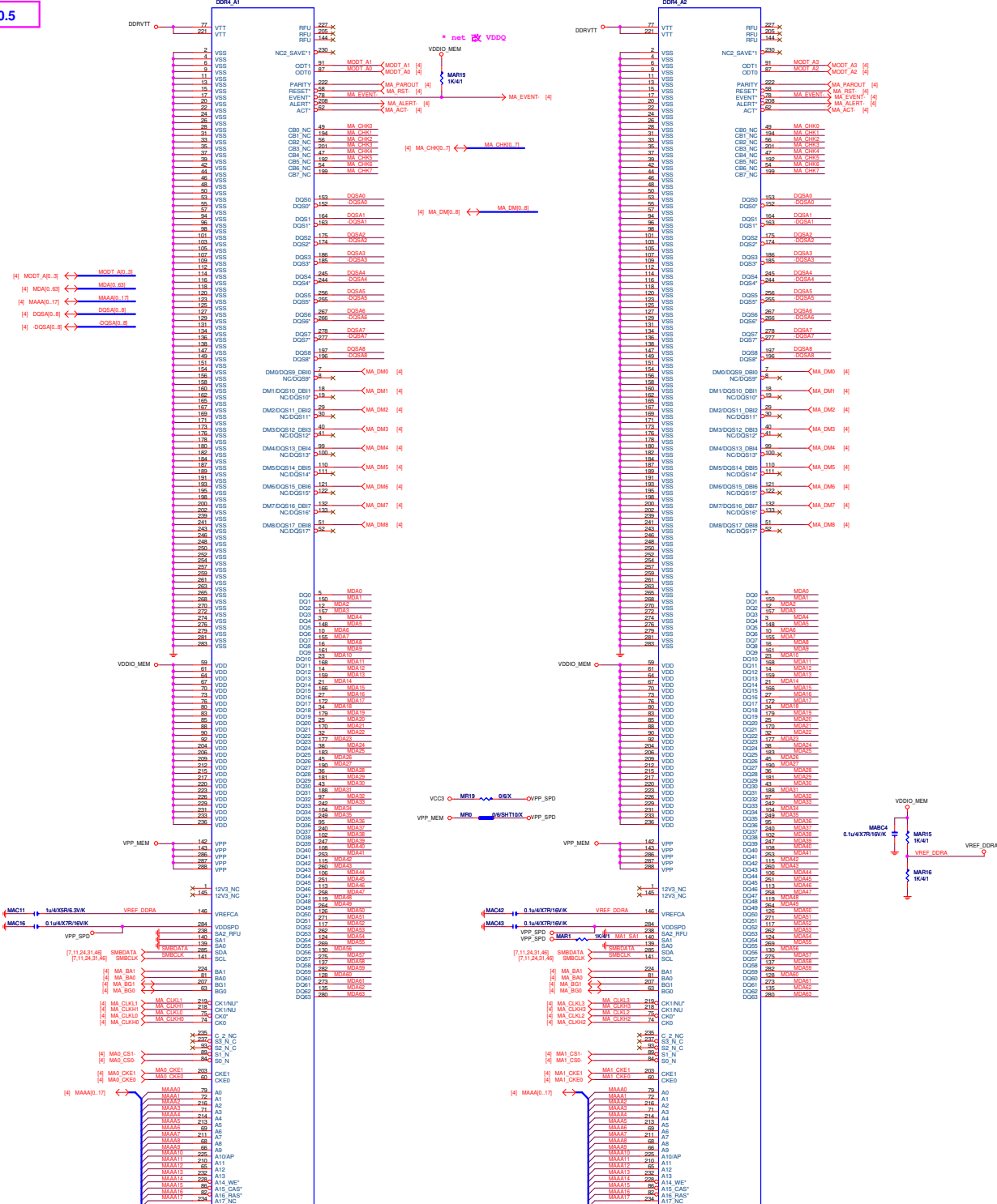
	SPI_CLK	LFRAME-	SYS_RST-	LPC_CLK0	LPC_CLK1
PULL HIGH	Internal clock mode	SPI ROM	Normal reset mode	PSP modify SPI page reg bits[24:24]	Use 48MHz crystal clock
PULL LOW	Extal clock mode	LPC ROM	Short reset mode	PSP not modify SPI page reg bits[24:24]	Use 100MHz extl clock input.

**Bule: default**



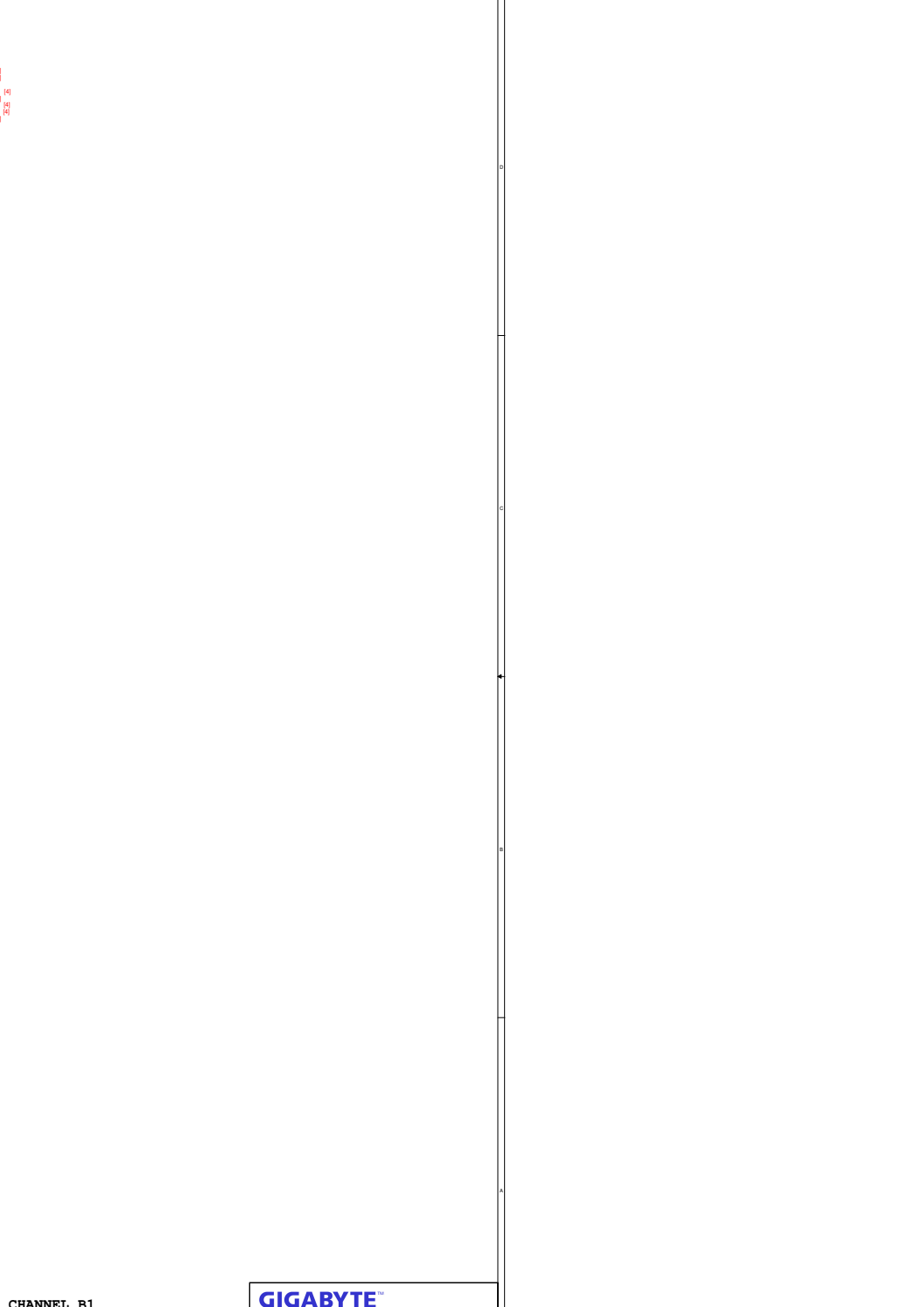
Single (256Mx1)  
# Layout colay 128Mx1



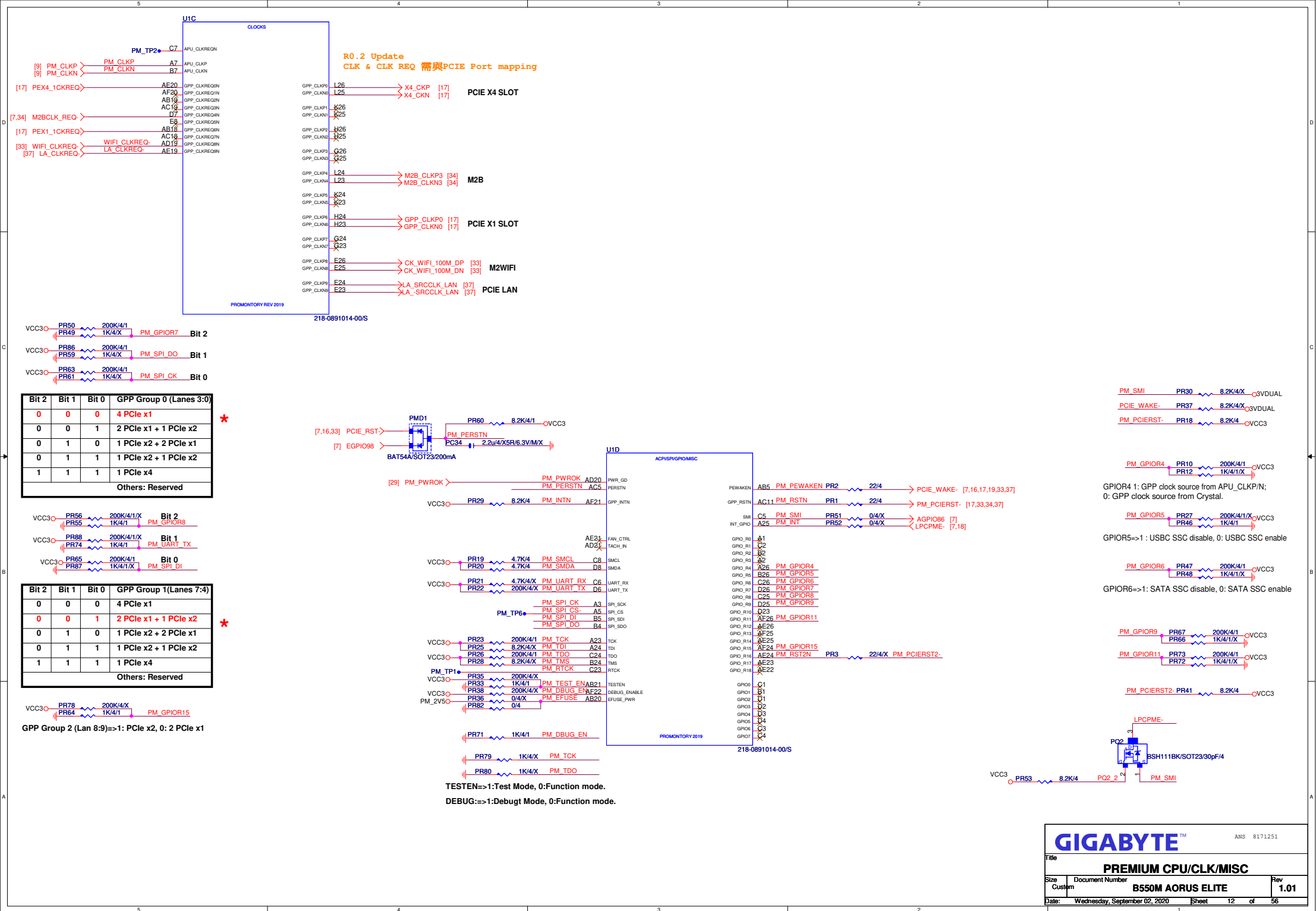




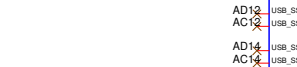
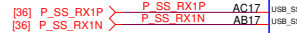
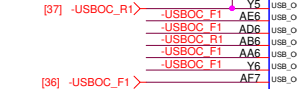
CHANNEL B0  
SA2:1=001



CHANNEL B1  
SA2:3=011

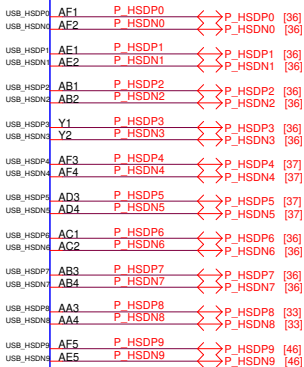


USB port power control 9:0  
(VCC3). Output.

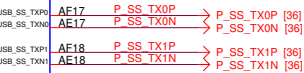


PROMONTORY REV 2019 218-0891014-00/S

USB32G2	USB20	USB_OC
0	0	0
1	1	1
USB32G1		
0	2	2
1	3	3
	4	4
	5	5
	6	6
	7	7
	8	7
	9	7



### USB 3.1 Gen 1



### USB 3.1 Gen 2



KB\_MS\_USB OK

KB\_MS\_USB OK

F\_USB30 OK

F\_USB30 OK

LAN\_USB OK

LAN\_USB OK

F\_USB20 OK

F\_USB20 OK

M2 WIFI OK

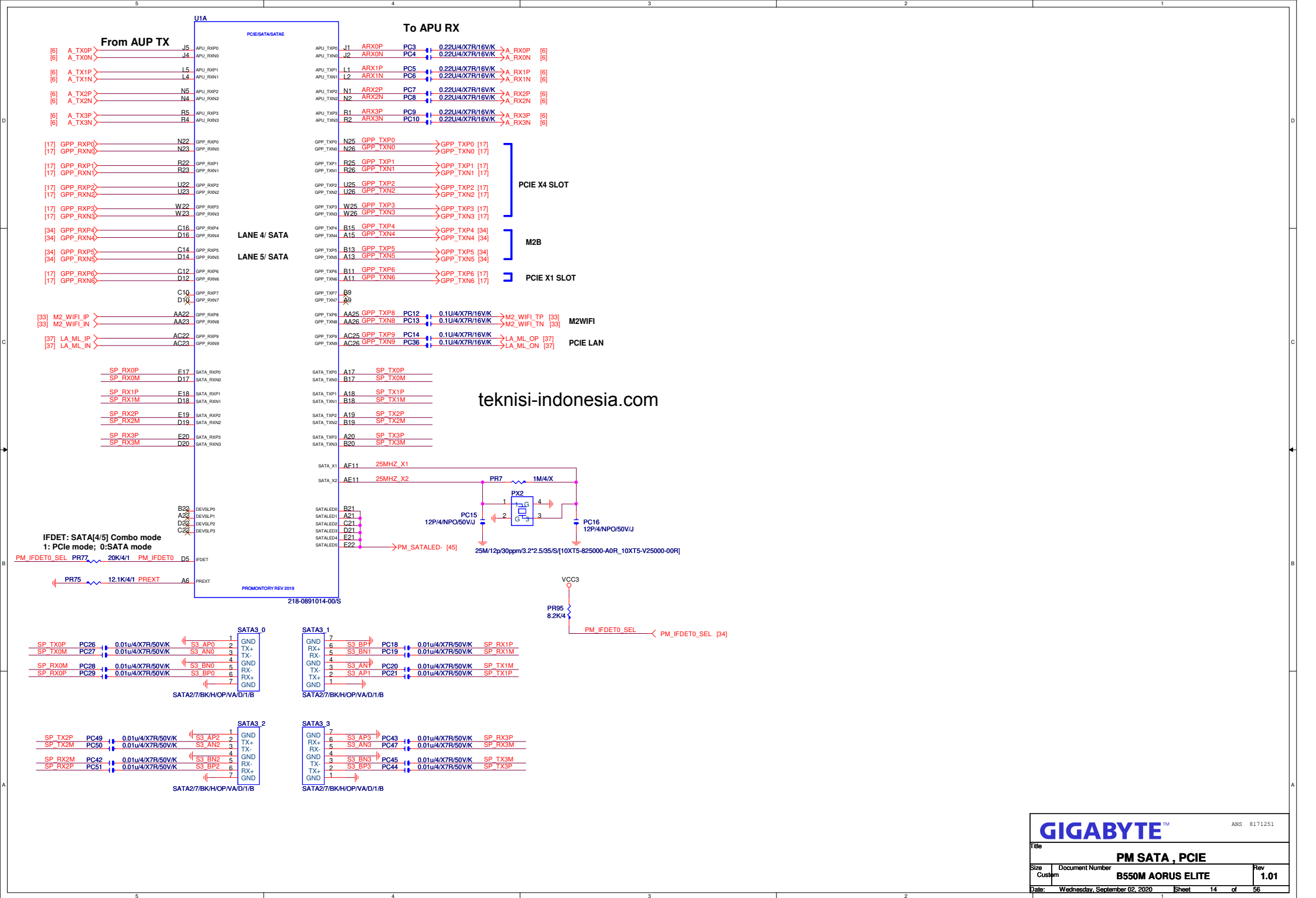
MCU OK

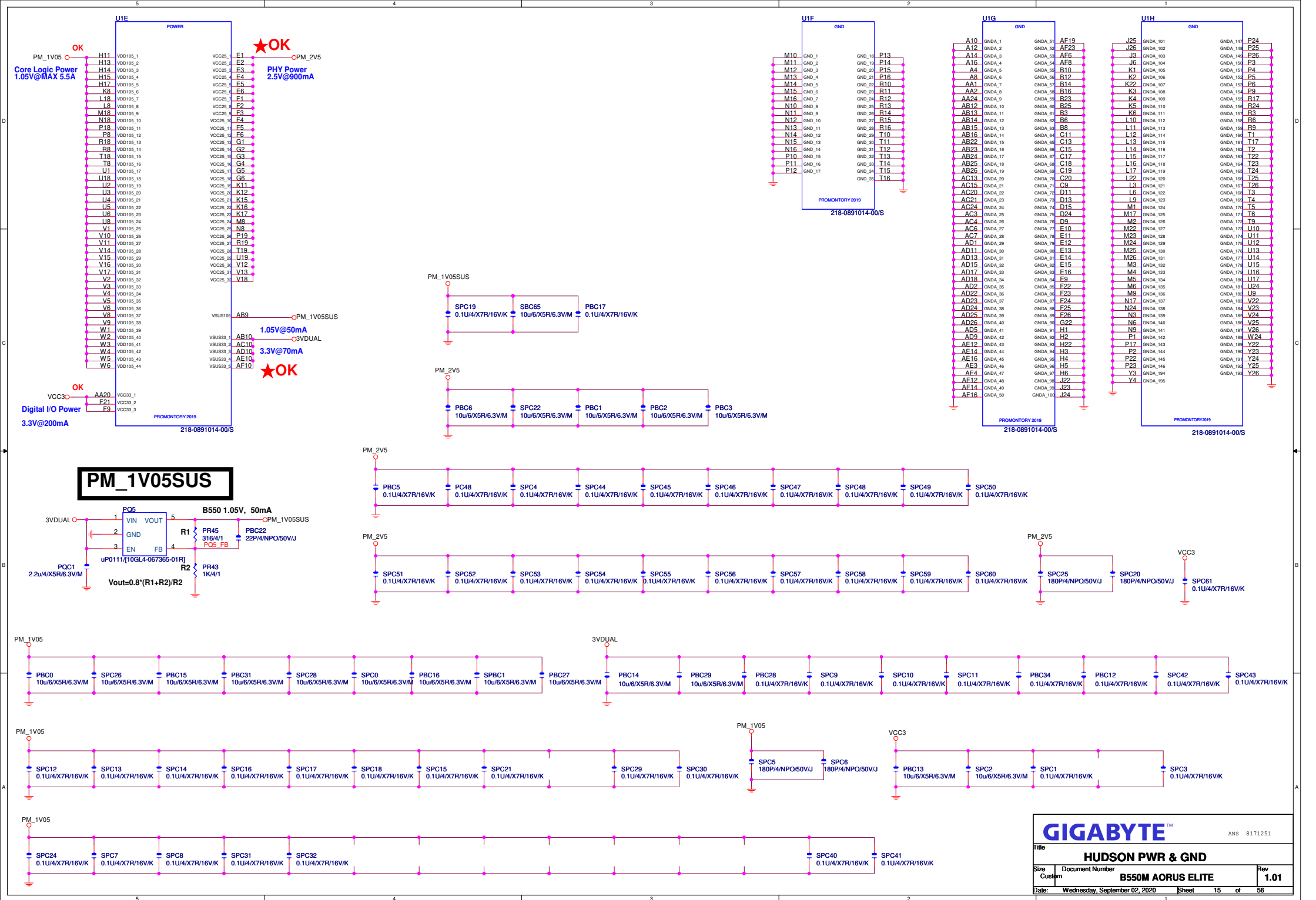
HSD 2 F\_USB30 OK

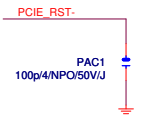
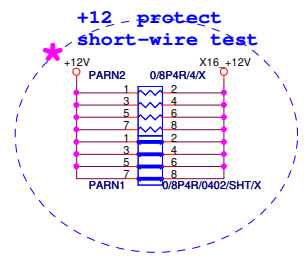
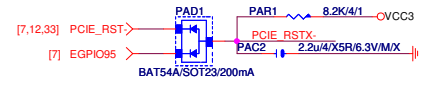
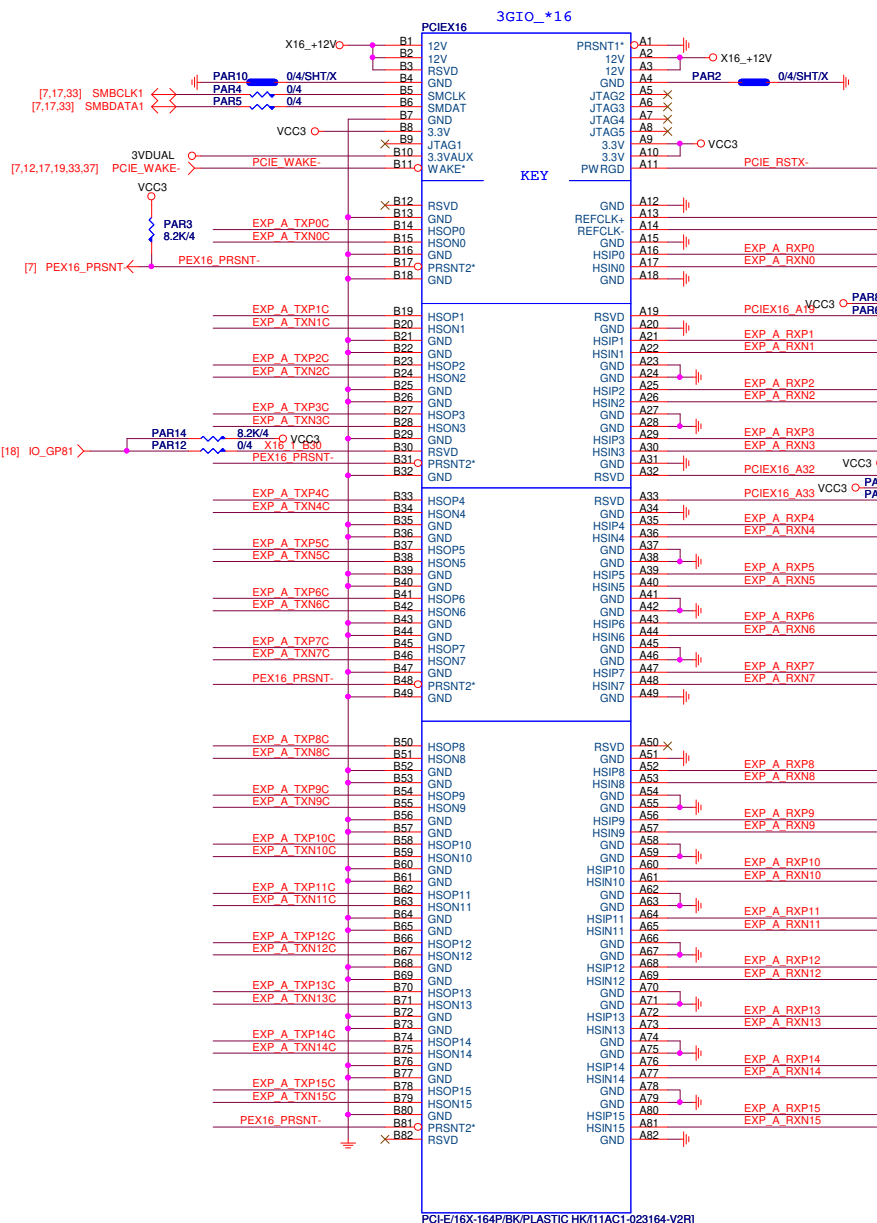
HSD 3 F\_USB30 OK

HSD 0

HSD 1

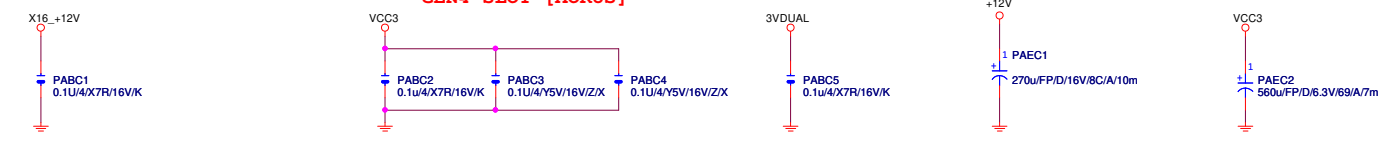






EXP A TXP0	PAC4	0.22u/4/X5R/6.3V/K	EXP A TXP0C
EXP A TXN0	PAC5	0.22u/4/X5R/6.3V/K	EXP A TXN0C
EXP A TXP1	PAC6	0.22u/4/X5R/6.3V/K	EXP A TXP1C
EXP A TXN1	PAC7	0.22u/4/X5R/6.3V/K	EXP A TXN1C
EXP A TXP2	PAC8	0.22u/4/X5R/6.3V/K	EXP A TXP2C
EXP A TXN2	PAC9	0.22u/4/X5R/6.3V/K	EXP A TXN2C
EXP A TXP3	PAC10	0.22u/4/X5R/6.3V/K	EXP A TXP3C
EXP A TXN3	PAC11	0.22u/4/X5R/6.3V/K	EXP A TXN3C
EXP A TXP4	PAC12	0.22u/4/X5R/6.3V/K	EXP A TXP4C
EXP A TXN4	PAC13	0.22u/4/X5R/6.3V/K	EXP A TXN4C
EXP A TXP5	PAC14	0.22u/4/X5R/6.3V/K	EXP A TXP5C
EXP A TXN5	PAC15	0.22u/4/X5R/6.3V/K	EXP A TXN5C
EXP A TXP6	PAC16	0.22u/4/X5R/6.3V/K	EXP A TXP6C
EXP A TXN6	PAC17	0.22u/4/X5R/6.3V/K	EXP A TXN6C
EXP A TXP7	PAC18	0.22u/4/X5R/6.3V/K	EXP A TXP7C
EXP A TXN7	PAC19	0.22u/4/X5R/6.3V/K	EXP A TXN7C
EXP A TXP8	PAC20	0.22u/4/X5R/6.3V/K	EXP A TXP8C
EXP A TXN8	PAC21	0.22u/4/X5R/6.3V/K	EXP A TXN8C
EXP A TXP9	PAC22	0.22u/4/X5R/6.3V/K	EXP A TXP9C
EXP A TXN9	PAC23	0.22u/4/X5R/6.3V/K	EXP A TXN9C
EXP A TXP10	PAC24	0.22u/4/X5R/6.3V/K	EXP A TXP10C
EXP A TXN10	PAC25	0.22u/4/X5R/6.3V/K	EXP A TXN10C
EXP A TXP11	PAC26	0.22u/4/X5R/6.3V/K	EXP A TXP11C
EXP A TXN11	PAC27	0.22u/4/X5R/6.3V/K	EXP A TXN11C
EXP A TXP12	PAC28	0.22u/4/X5R/6.3V/K	EXP A TXP12C
EXP A TXN12	PAC29	0.22u/4/X5R/6.3V/K	EXP A TXN12C
EXP A TXP13	PAC30	0.22u/4/X5R/6.3V/K	EXP A TXP13C
EXP A TXN13	PAC31	0.22u/4/X5R/6.3V/K	EXP A TXN13C
EXP A TXP14	PAC32	0.22u/4/X5R/6.3V/K	EXP A TXP14C
EXP A TXN14	PAC33	0.22u/4/X5R/6.3V/K	EXP A TXN14C
EXP A TXP15	PAC34	0.22u/4/X5R/6.3V/K	EXP A TXP15C
EXP A TXN15	PAC35	0.22u/4/X5R/6.3V/K	EXP A TXN15C

EXP A RXP0..15]	>>>EXP_A_RXP[0..15]	[6]
EXP A RXN0..15]	>>>EXP_A_RXN[0..15]	[6]
EXP A TXP0..15]	>>>EXP_A_TXP[0..15]	[6]
EXP A TXN0..15]	>>>EXP_A_TXN[0..15]	[6]



**GIGABYTE**<sup>TM</sup>

**PCI EXPRESS X 16**

Size Custom

Document Number

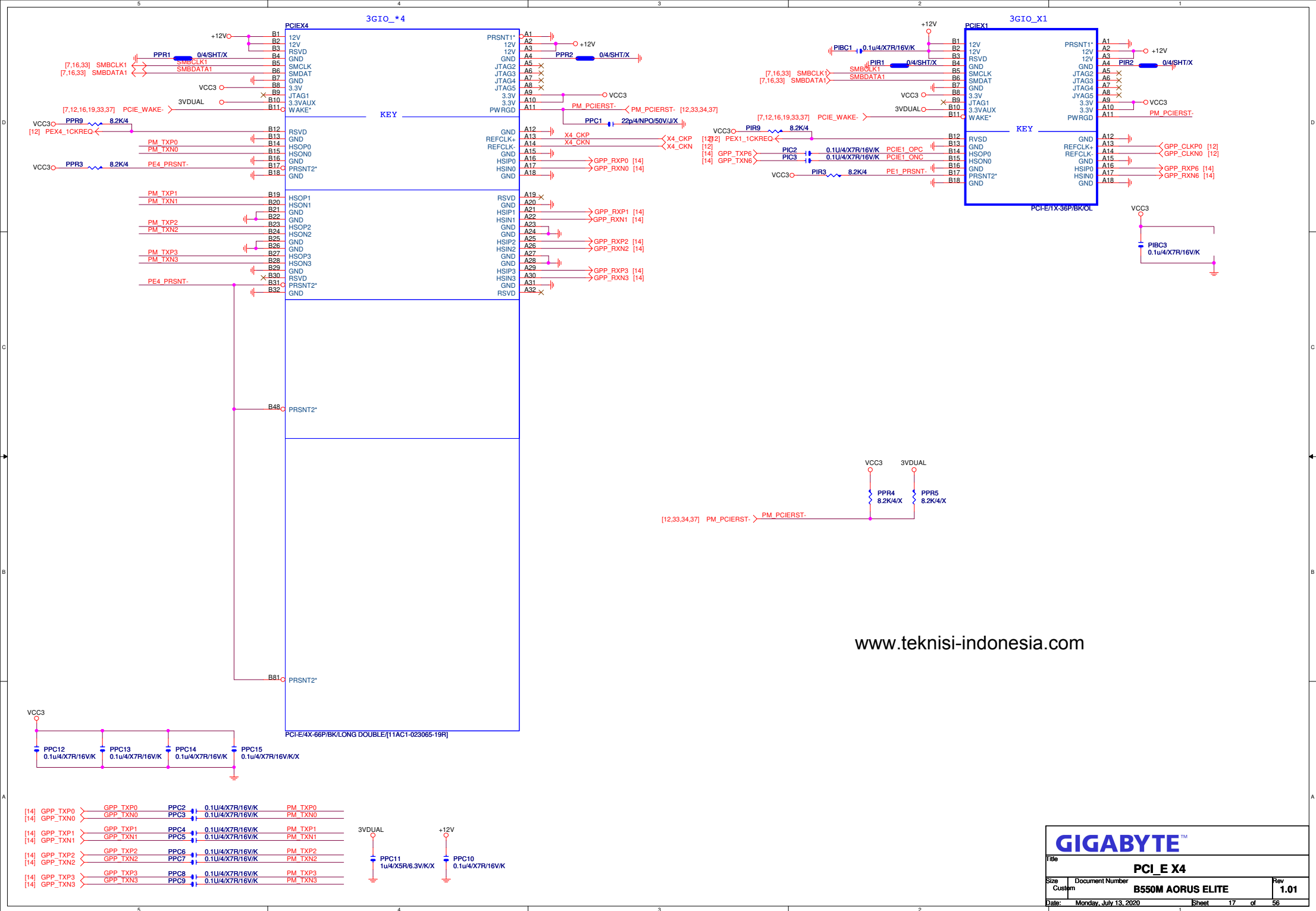
B550M AORUS ELITE

Date: Monday, July 13, 2020

Sheet 16 of 56

Rev 1.01

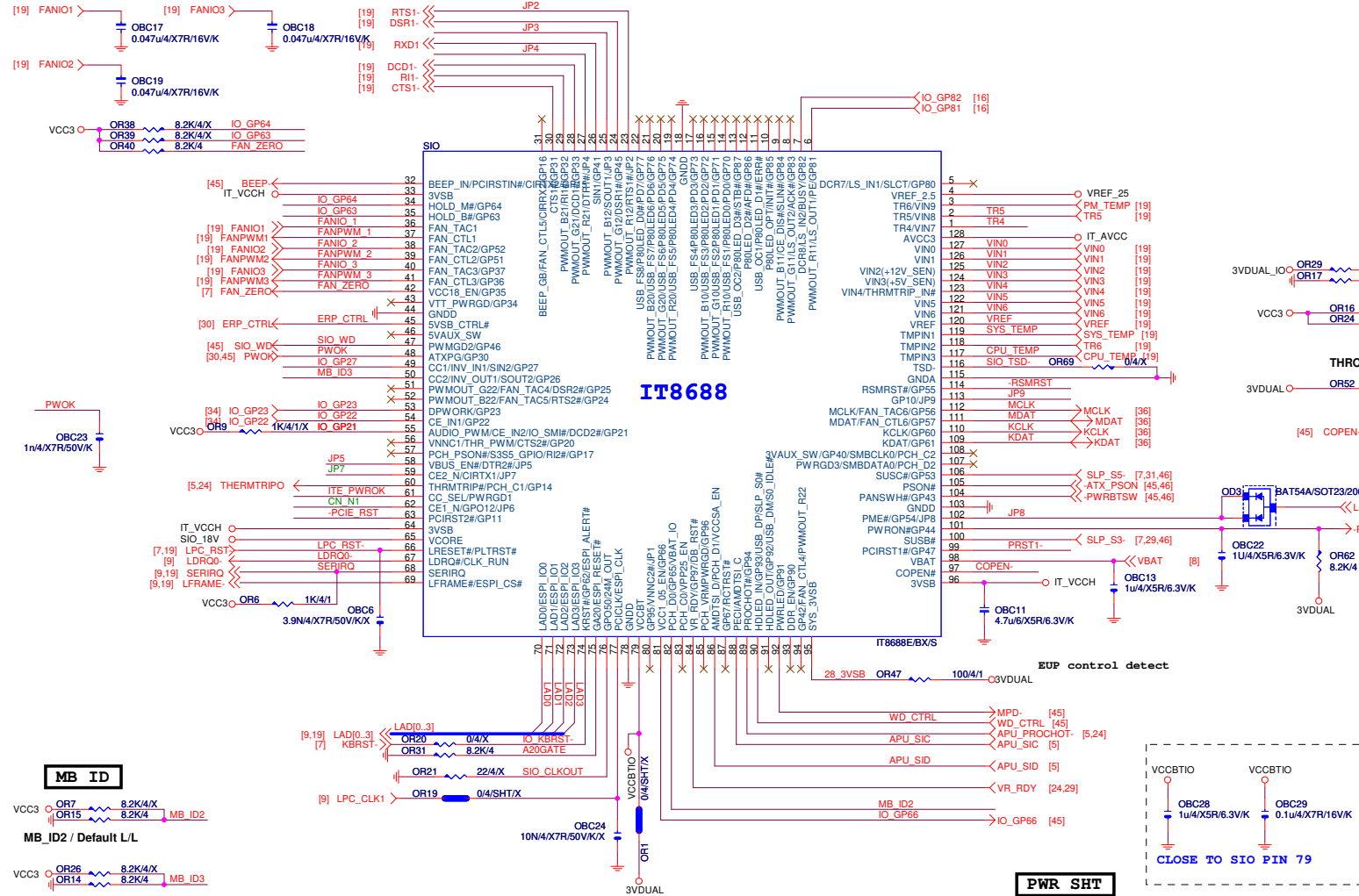




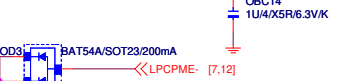
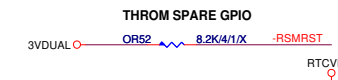
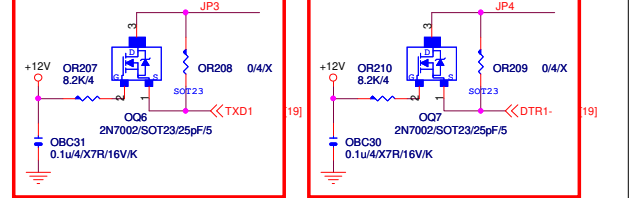
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GIGABYTE™			
Title			
PCI E X4			
Size	Document Number	Rev	
Custom	B550M AORUS ELITE	1.01	
Date:	Monday, July 13, 2020	Sheet	17 of 56

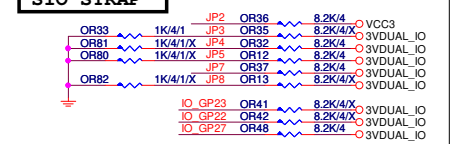
# SIO IT8628CX REV:1.09



## for LPC/eSPI power mode



## SIO STRAP



JP2	1	Disable WDT to rest PWROK
JP2	0	Enable WDT to rest PWROK
JP3	1	Dual-BIOS CS pin mode select bit "0"
JP3	0	See the below table
JP4	1	LPC/eSPI power VCCBT = 3.3V
JP4	0	LPC/eSPI power VCCBT = 1.8V
JP5	1	LPC I/F
JP5	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
JP6	0	Disable Dual BIOS Function (for GigaByte Only)
JP7	1	Dual-BIOS CE pin mode select bit "1"
JP7	0	See the below table
JP7	1 1	CE pin disable (Hold pin mode)
JP7	1 0	CE mode 1
JP3	0 1	CE mode 2
JP3	0 0	CE mode 3

**GIGABYTE™**

**ITE 8686 LPC IO, TPM, KB/MS**

Title

Document Number

Rev

B550M AORUS ELITE

1.01

Size

Custom

Monday, July 13, 2020

Sheet 18 of 56

FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
OPT_FAN or SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP	PIN56
PROCHOT	PIN89

**DUAL BIOS OPT STRAP**

OR58 上件/OR56 不上件 SINGLE BIOS,

OR58 不上件/OR56 上件 DUAL BIOS

**EMI**

OBC27

0.01u4/X7R/50V/K

**Power leakage**

**SIO\_18V**

internal power pin, max 22nF cap

SIO\_18V

OBC4

0.1u4/X7R/16V/K

OBC5

0.1u4/X7R/16V/K

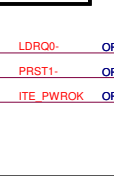
**ITE COMMENTS**

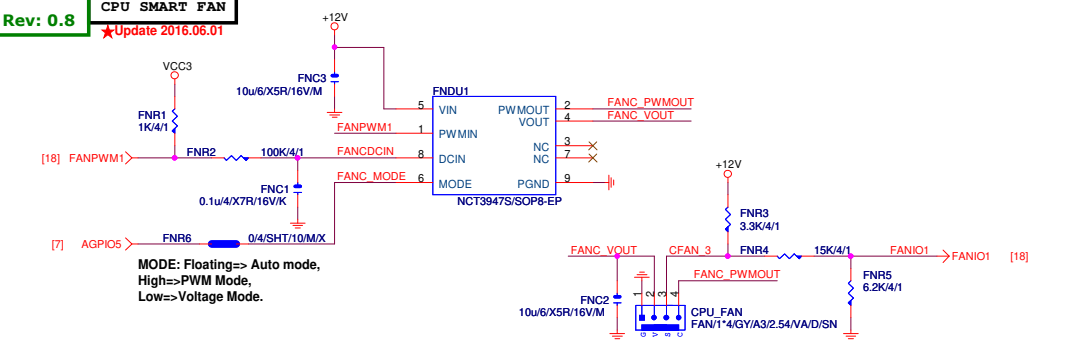
REGULATOR AP7365-WG-7 DII10GL4-067365-01R

Vout=0.8\*(R1+R2)/R2

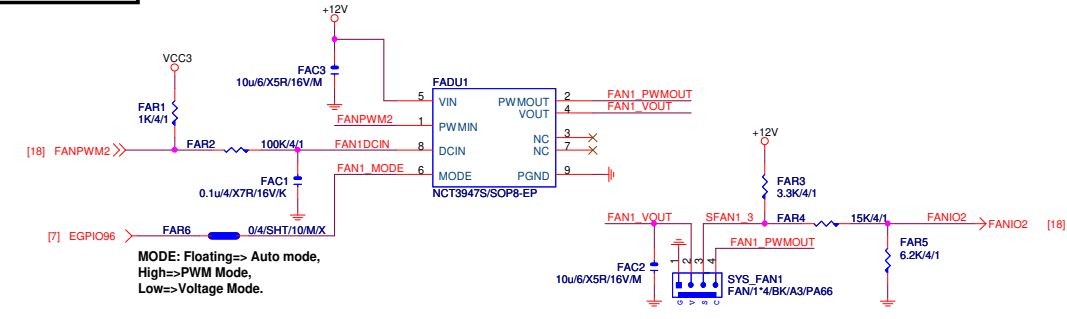
For Erp patch

## SIO PU

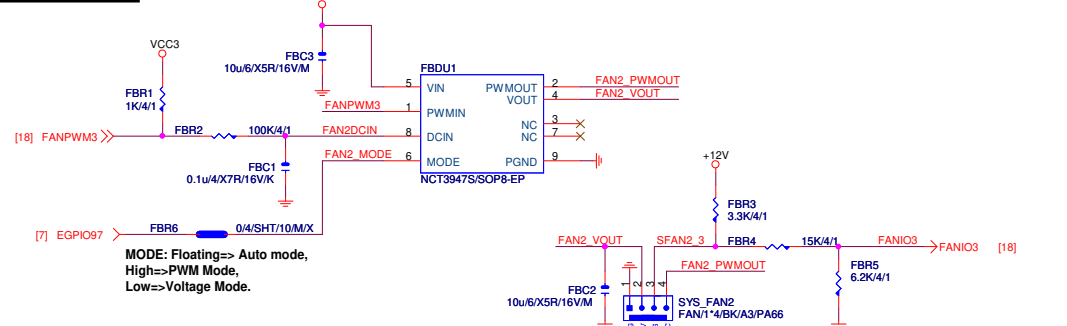




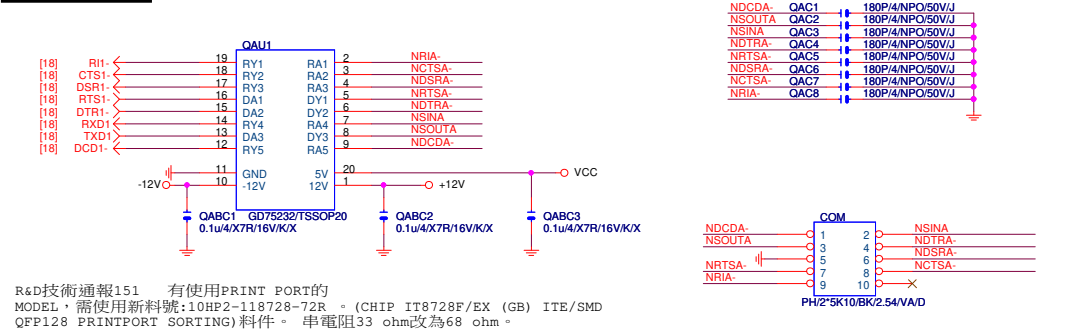
SYSTEM FAN1



SYSTEM FAN2

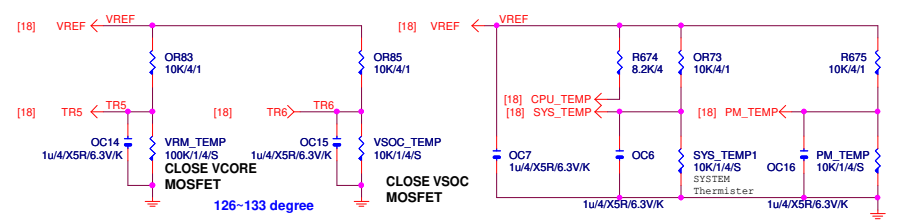


COM PORT

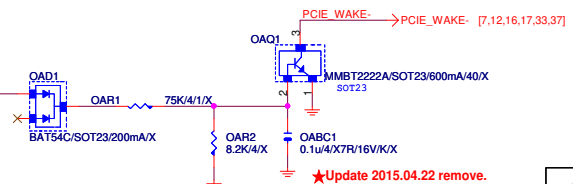
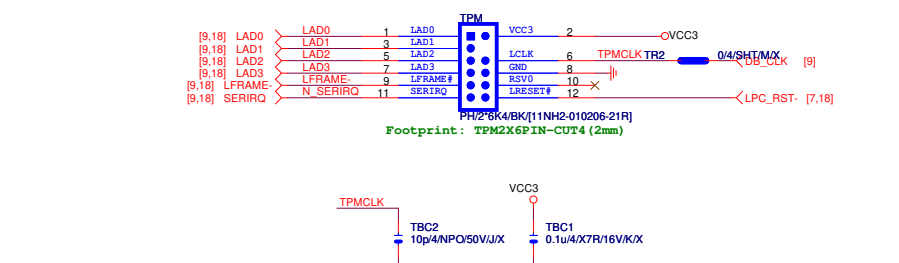
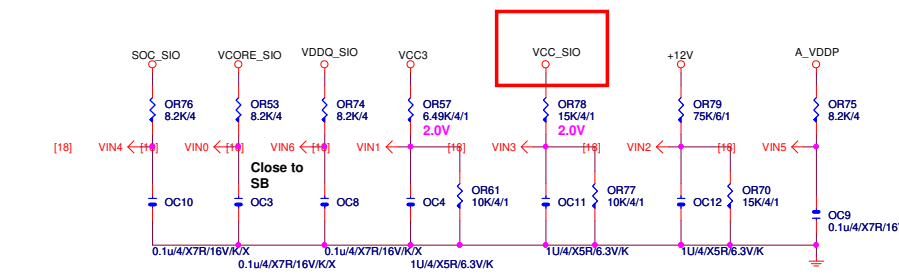


R&D技術通報151 有使用PRINT PORT的  
MODEL, 需使用新料號:10HP2-118728-72R (CHIP IT8728F/EX (GB) ITE/SMD  
QFP128 PRINTPORT SORTING)料件。串電阻33 ohm改為68 ohm。

Hardware Monitor circuits - Temperature



Hardware Monitor circuits - VOLTAGE



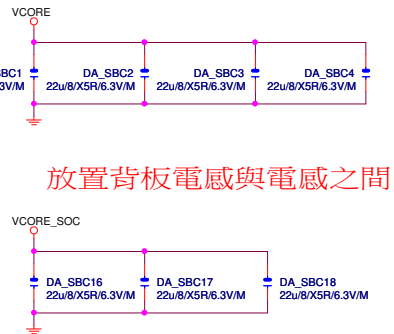
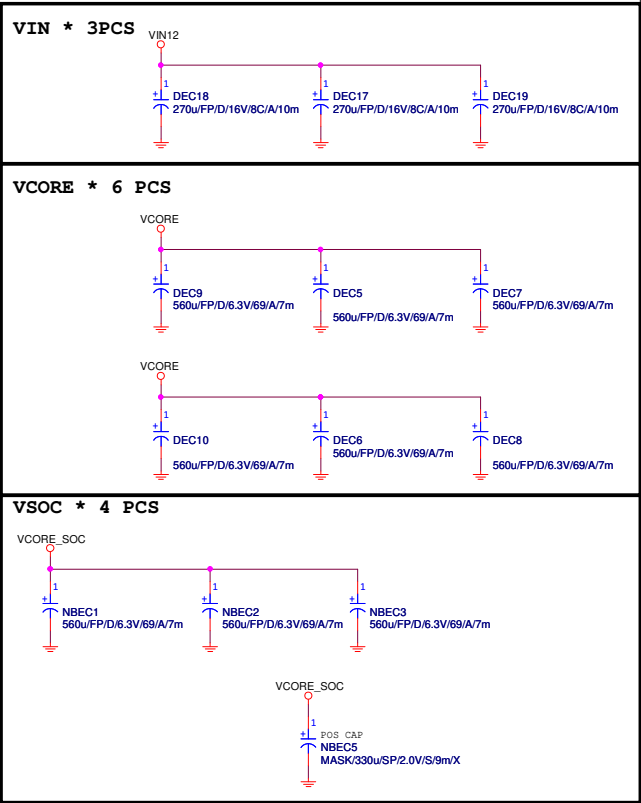
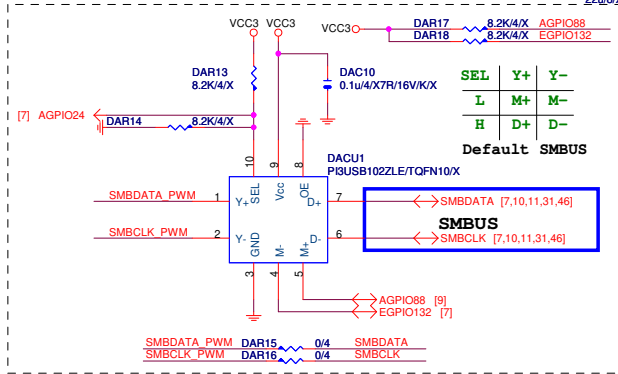
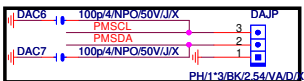
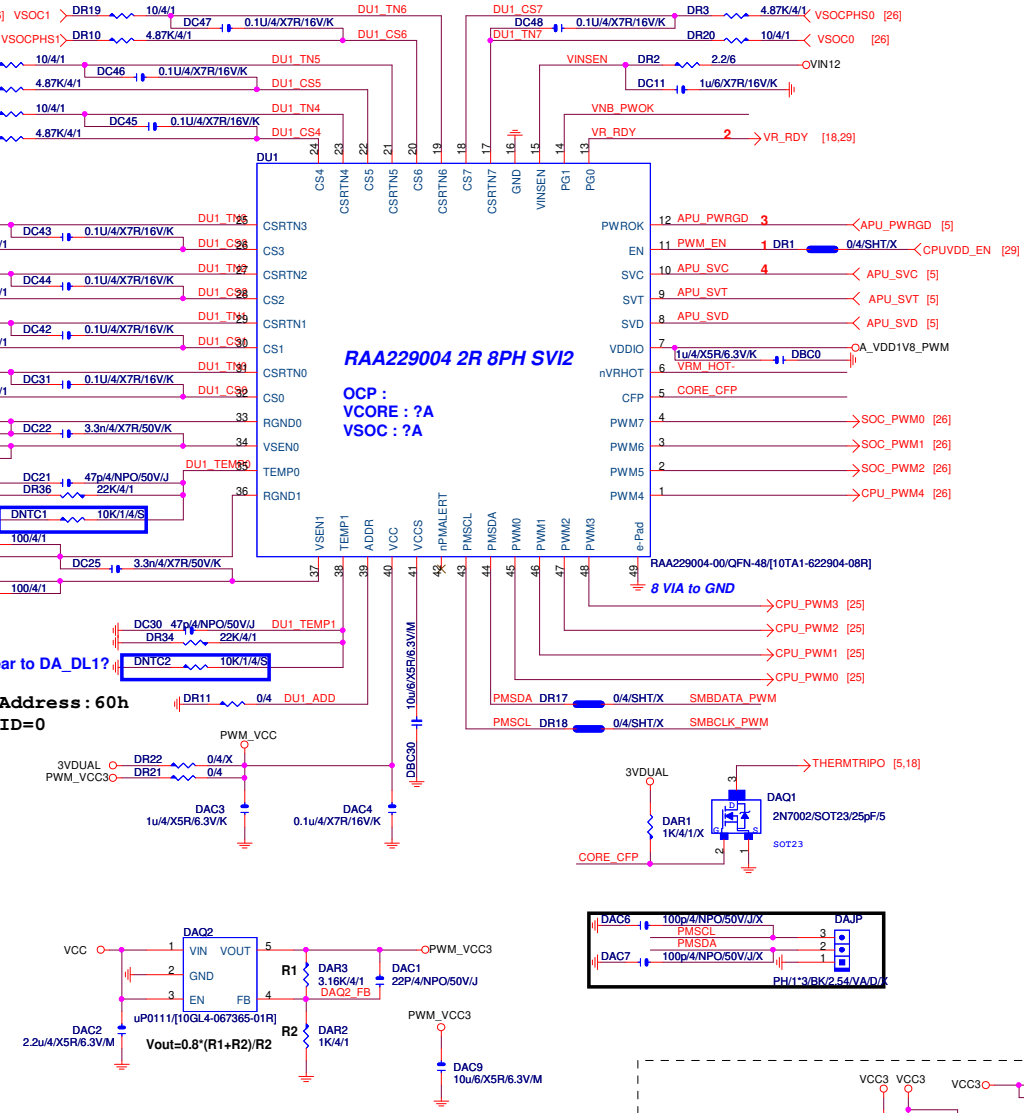
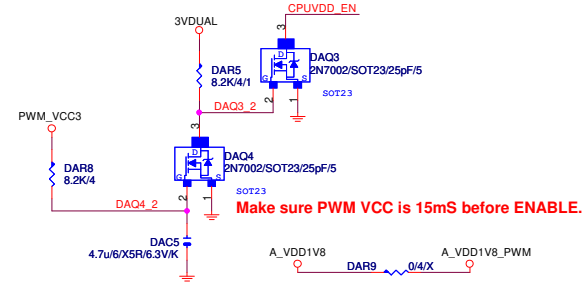
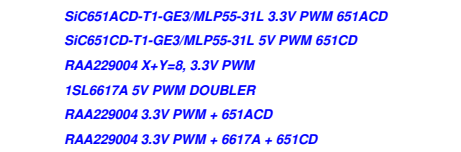
**GIGABYTE**™

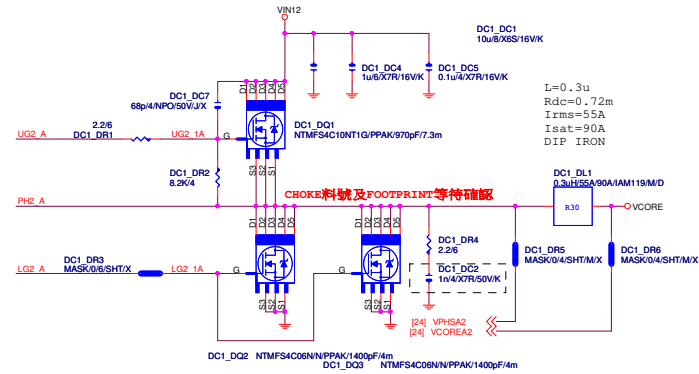
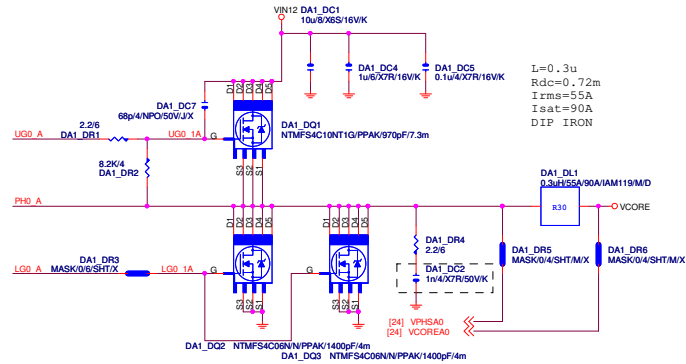
Title: **CKG, HWM, TPM, THB**

Size: **B550M AORUS ELITE**

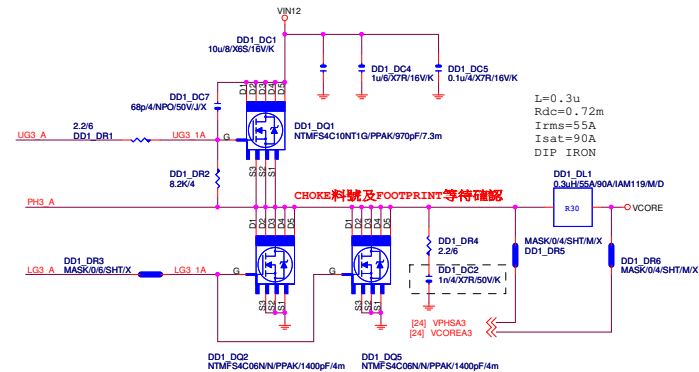
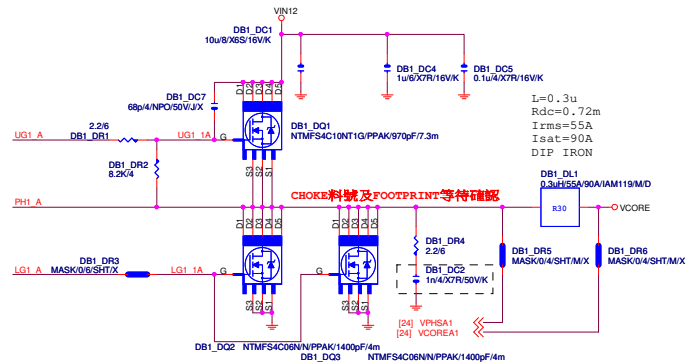
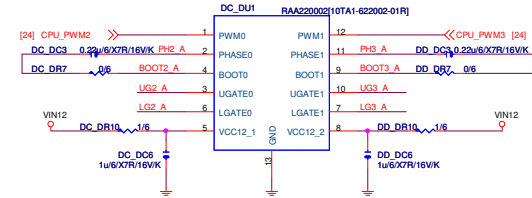
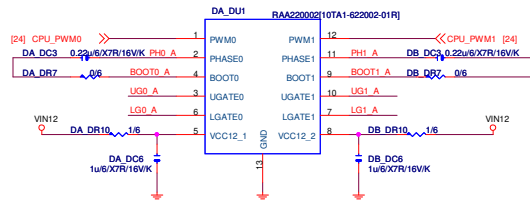
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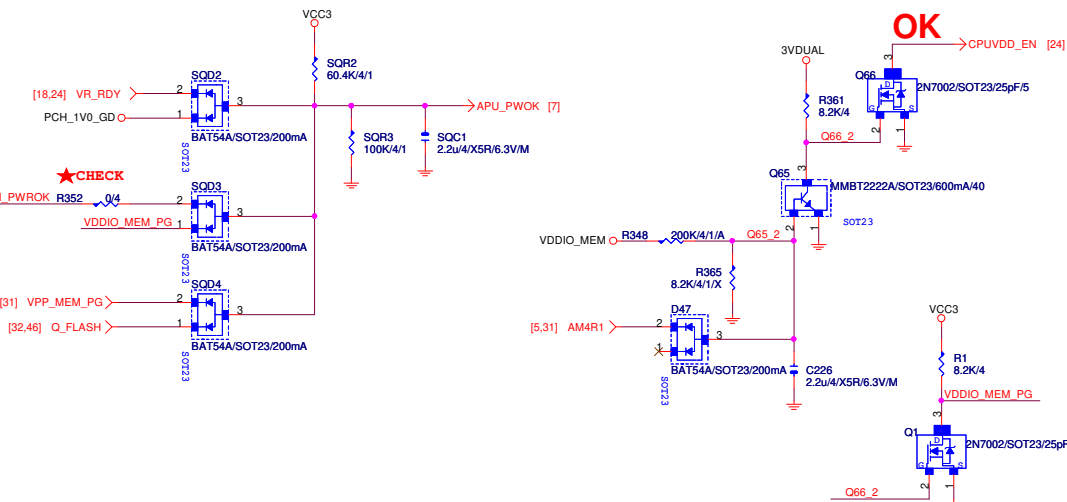
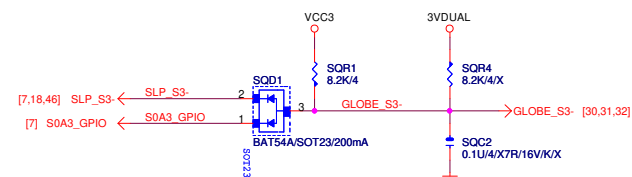
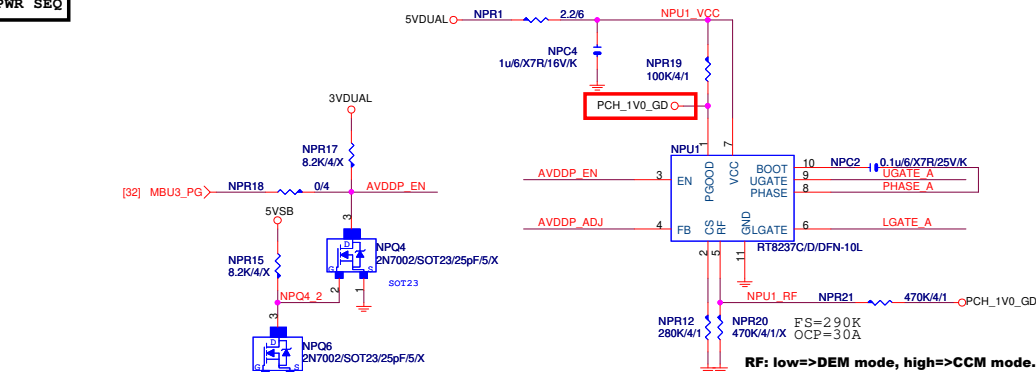
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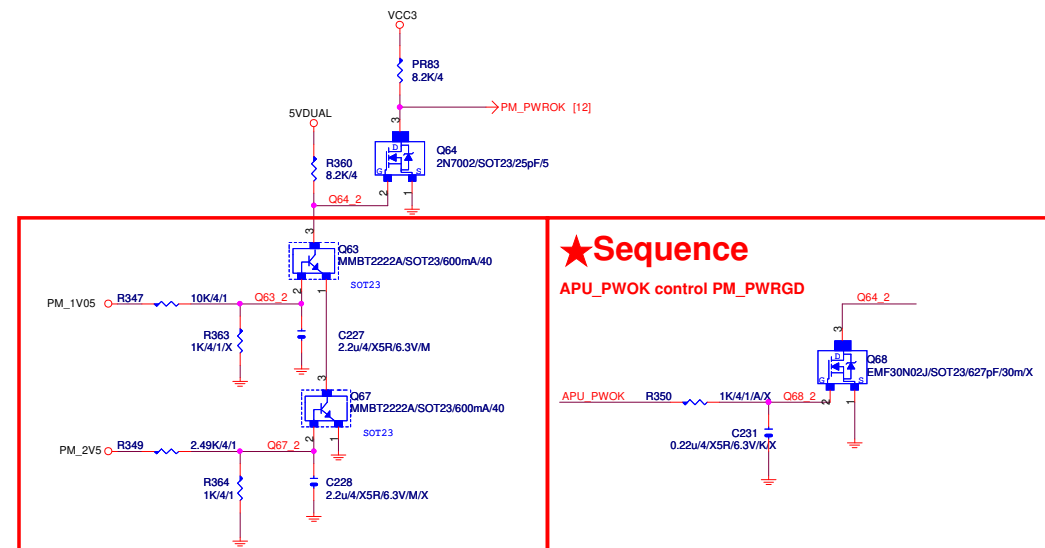
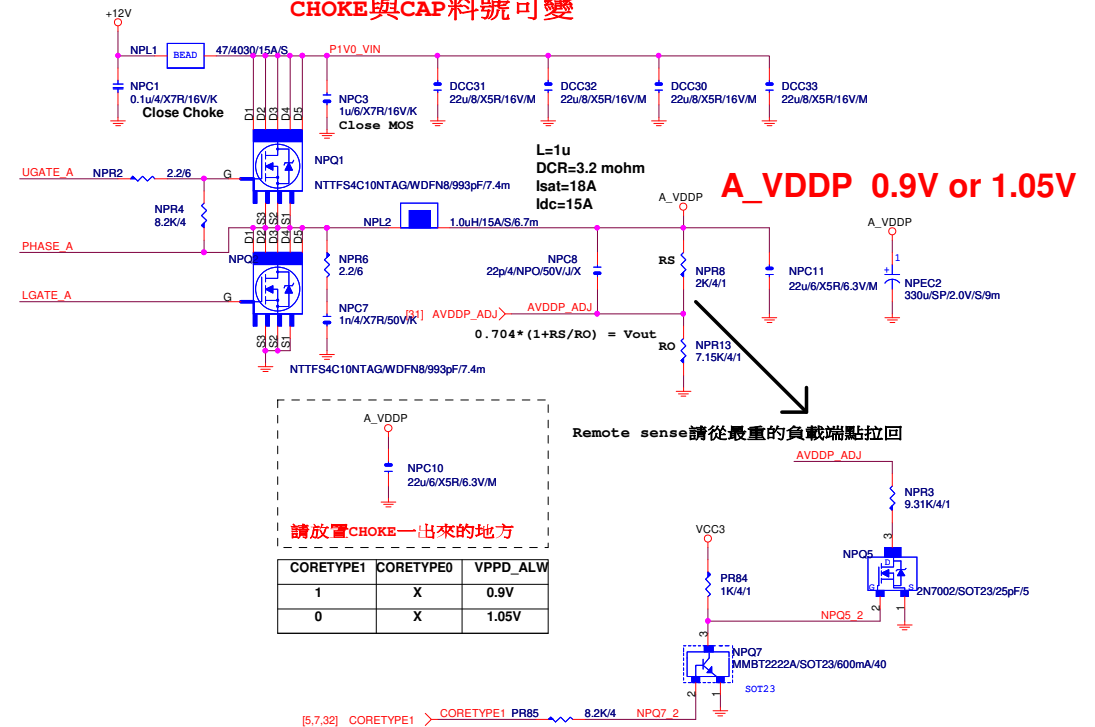
**GIGABYTE™**

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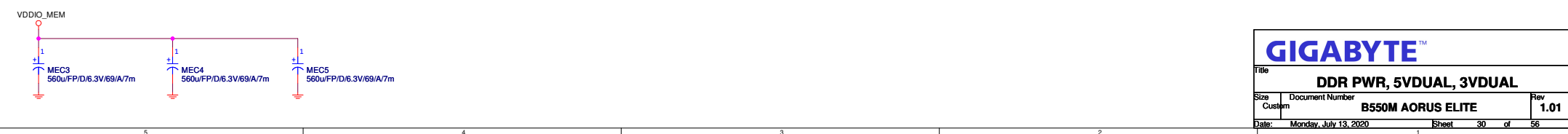
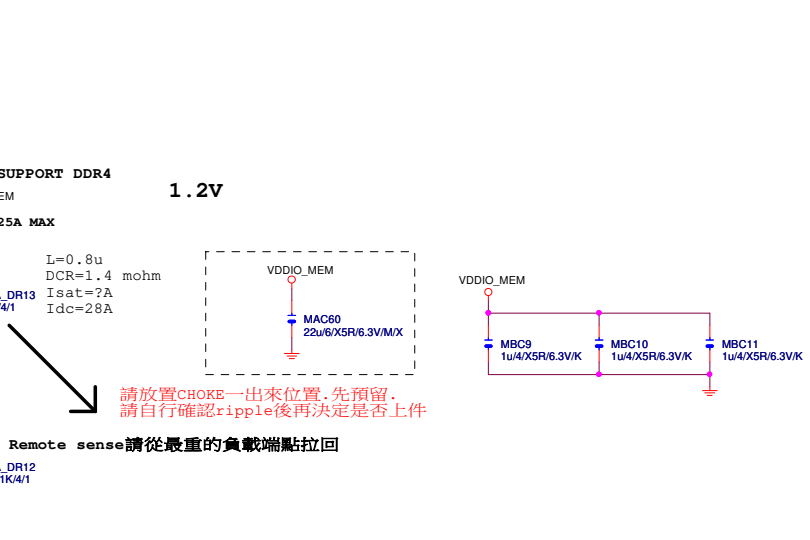
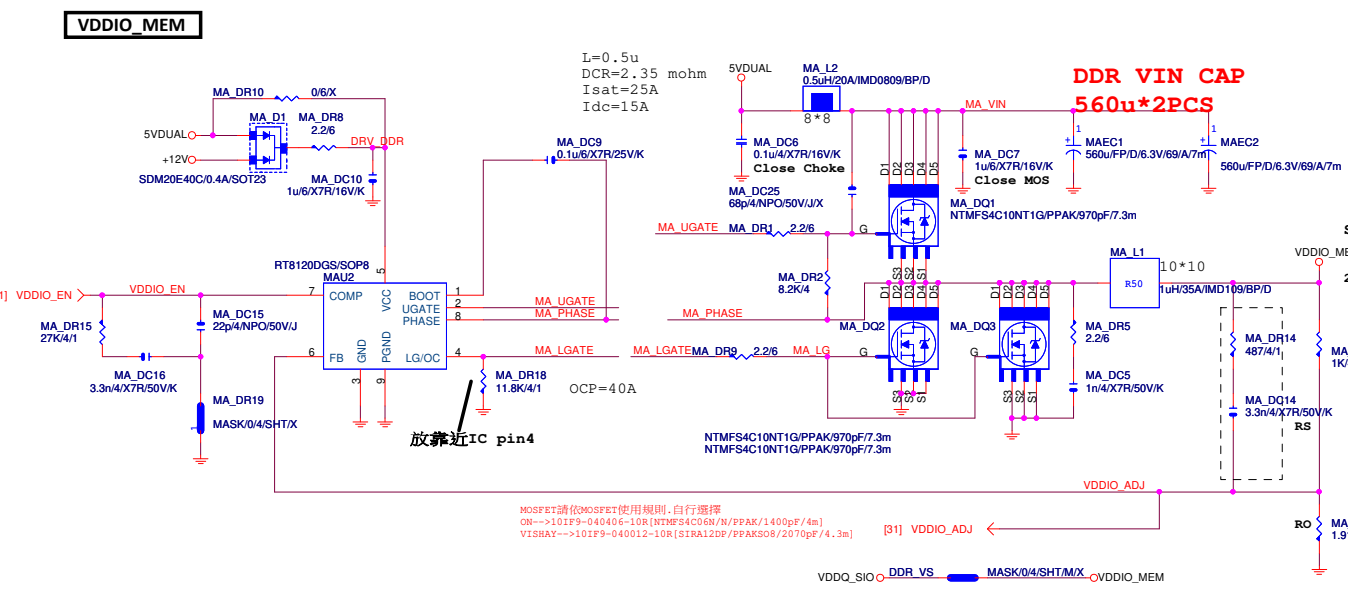
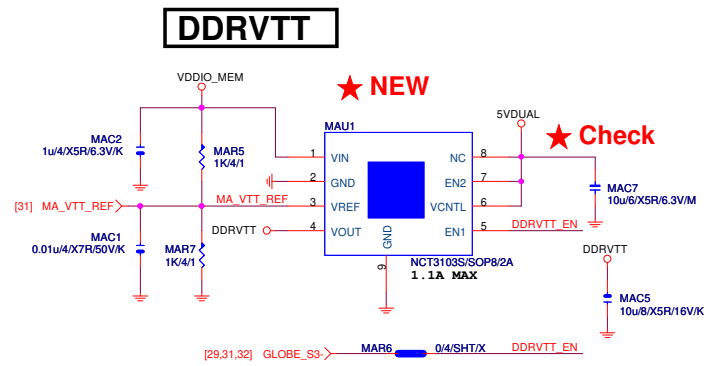
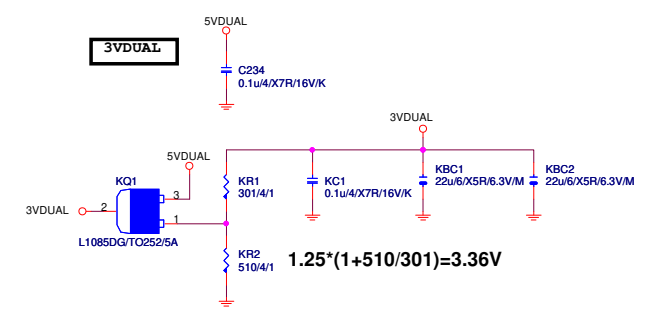
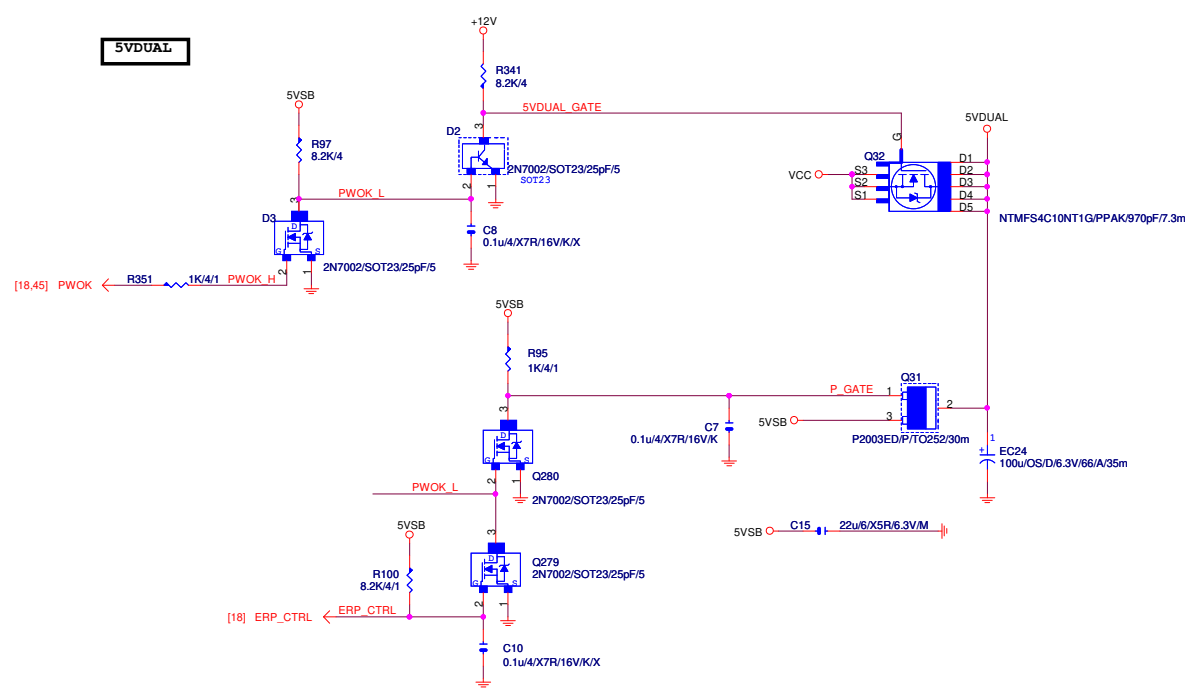


## CHOKE與CAP料號可變

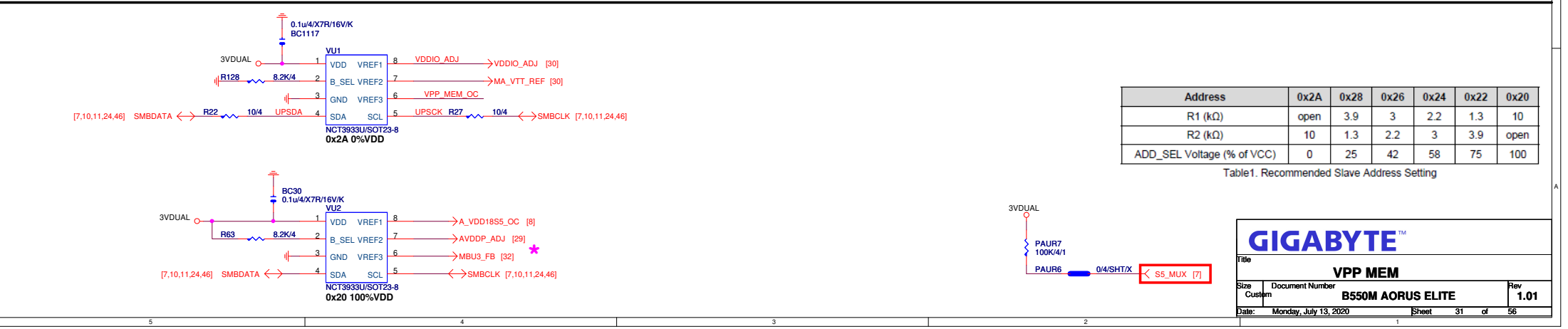
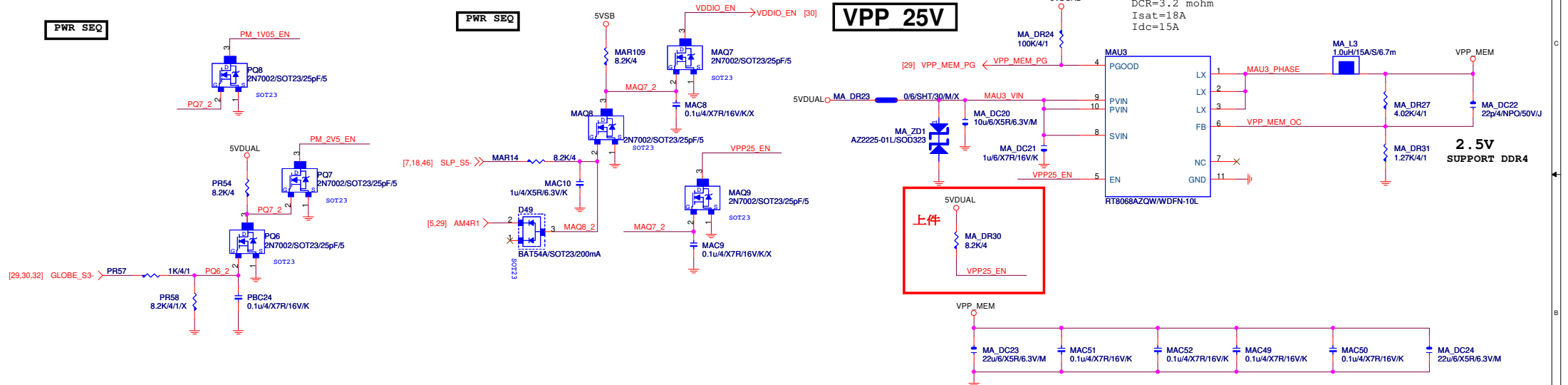
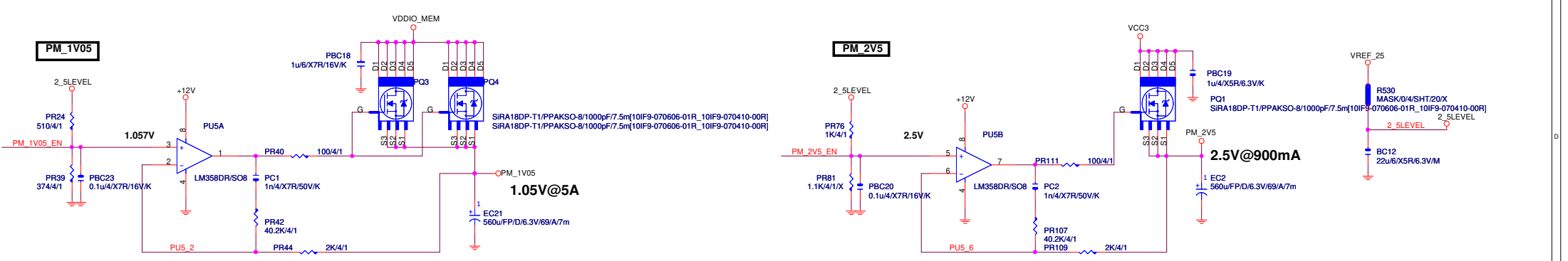


**GIGABYTE**™

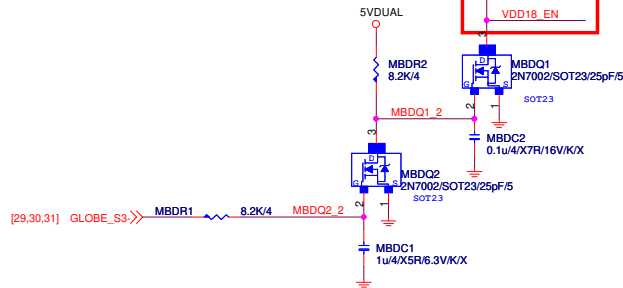
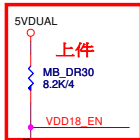
POWER SEQUENCE		
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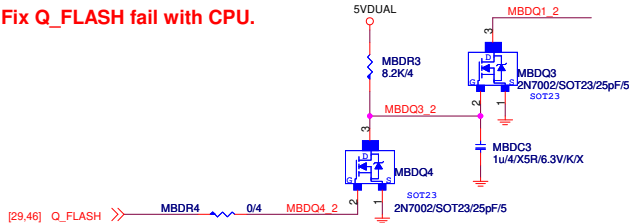




PWR\_SEQ

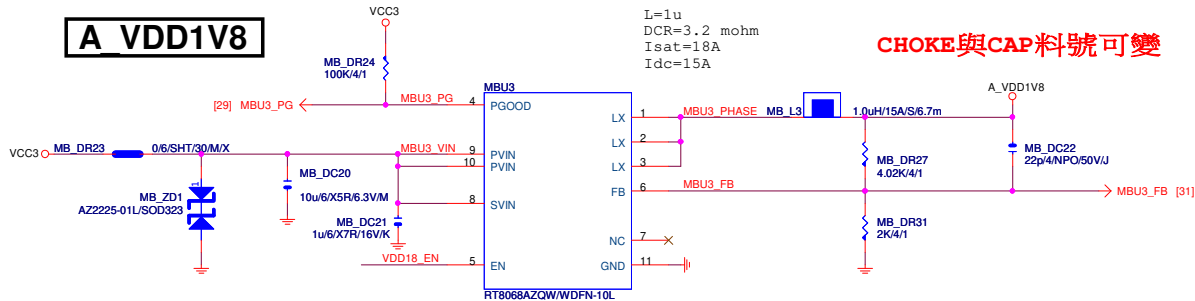


Fix Q\_FLASH fail with CPU.

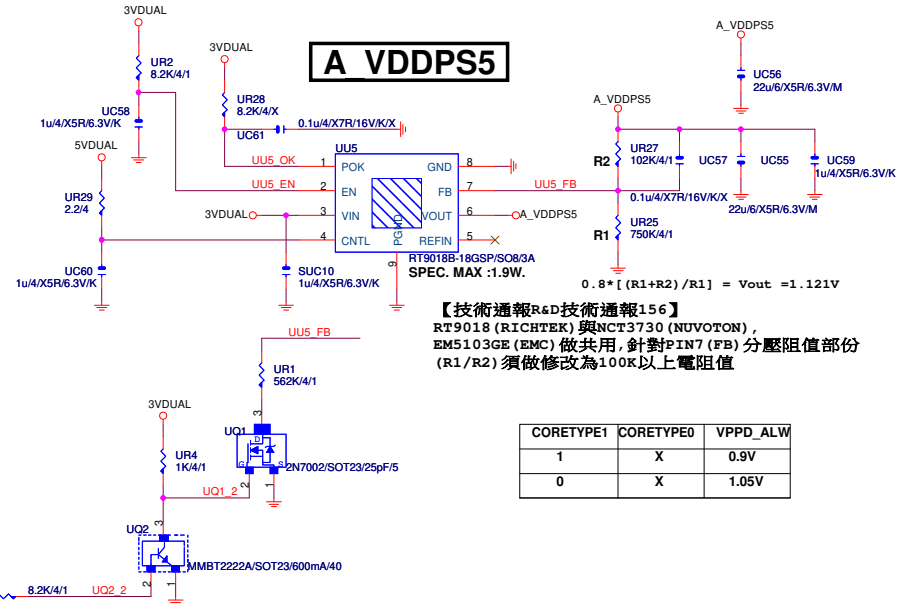


REV:0.4

A VDD1V8

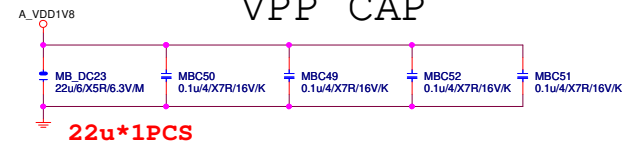


A VDDPS5



CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

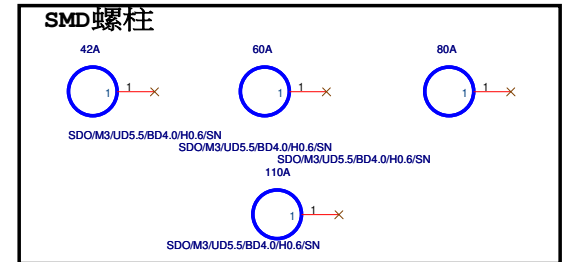
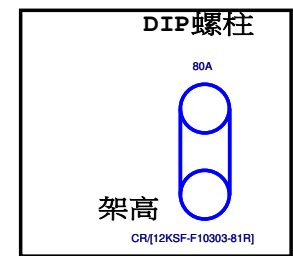
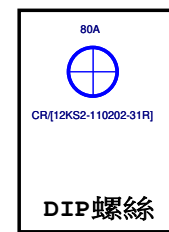
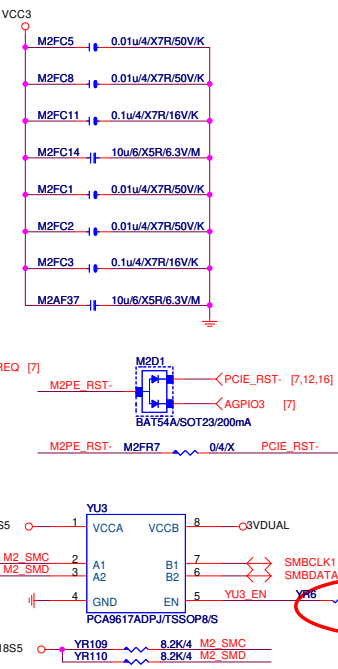
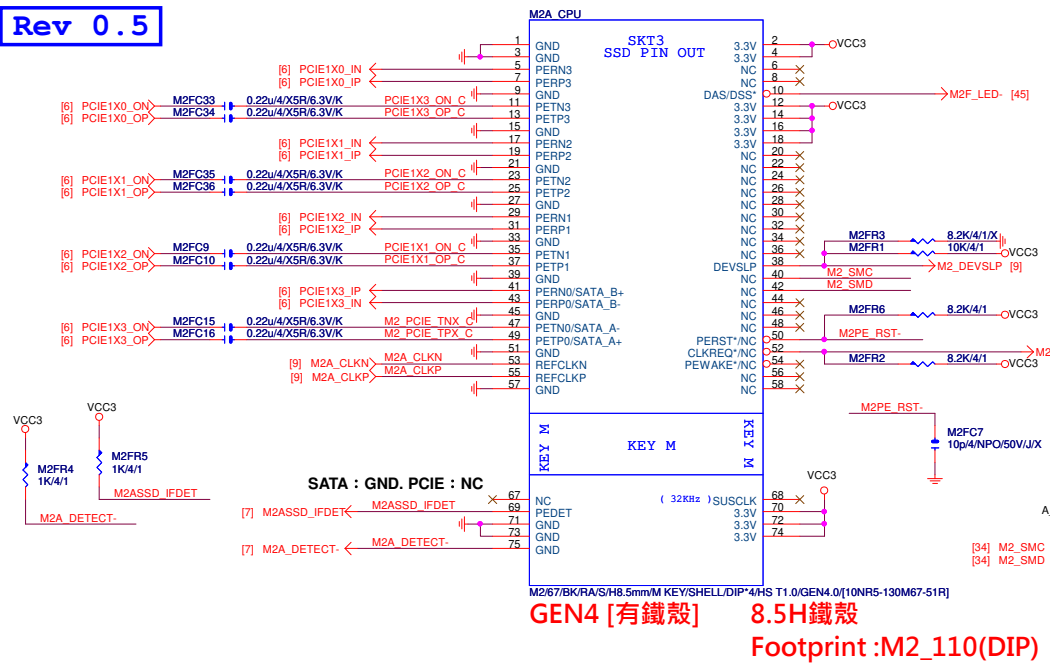
VPP CAP



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Rev 0.5



GEN4 [有鐵殼]      8.5H鐵殼  
Footprint :M2\_110(DIP)

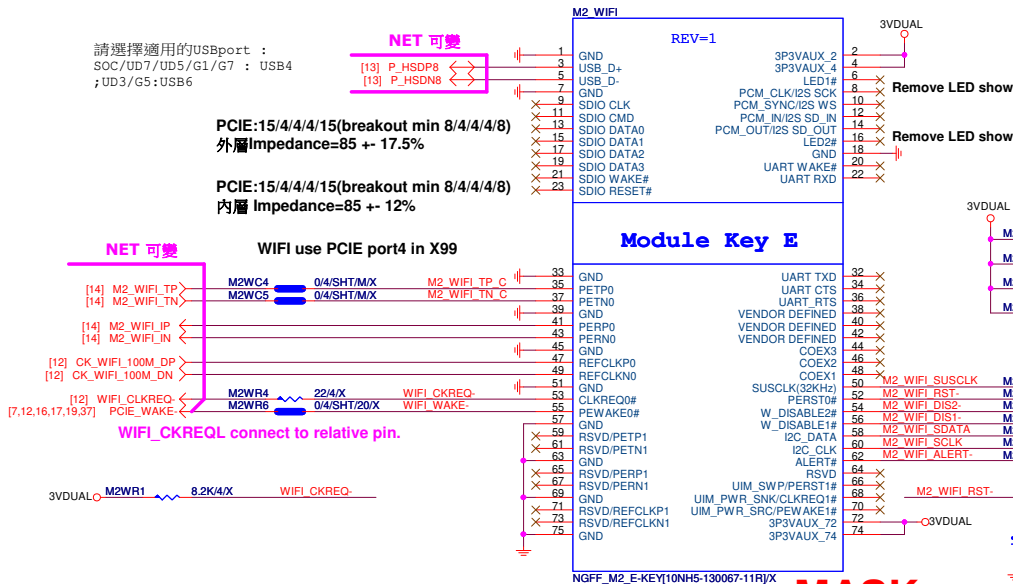
Rev: 0.2

請選擇適用的USBport：  
SOC/UD7/UD5/G1/G7：USB4  
;UD3/G5:USB6

PCIE:15/4/4/15(breakout min 8/4/4/8)  
外層Impedance=85 +- 17.5%

PCIE:15/4/4/15(breakout min 8/4/4/8)  
内層 Impedance=85 +- 12%

### WIFI use PCIE port4 in X99



## Footprint Notice.

★Update 2015-07-22  
★Footprint for  
直立式 SMD:  
WIFI-EKEY

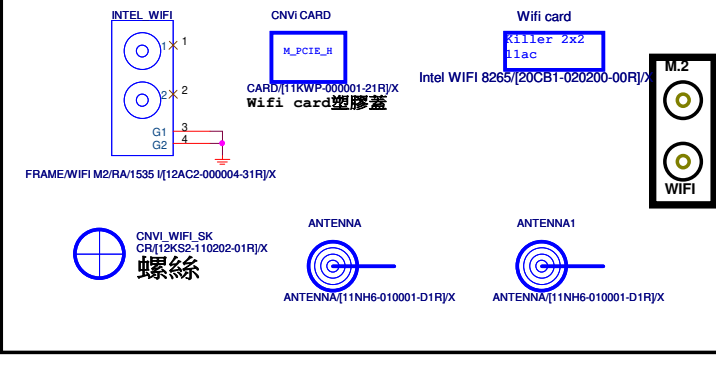
**MASK**  
Footprint Notice.

★Update 2015-07-22  
★Footprint for  
橫鎖式SMD: NGFF-E-75P-2

**FOR M.2 WIFI MODULE @ REAR PANEL**

★Update 2015-02-11

一套WIFI MODULE包含外框+WIFI CARD+天線

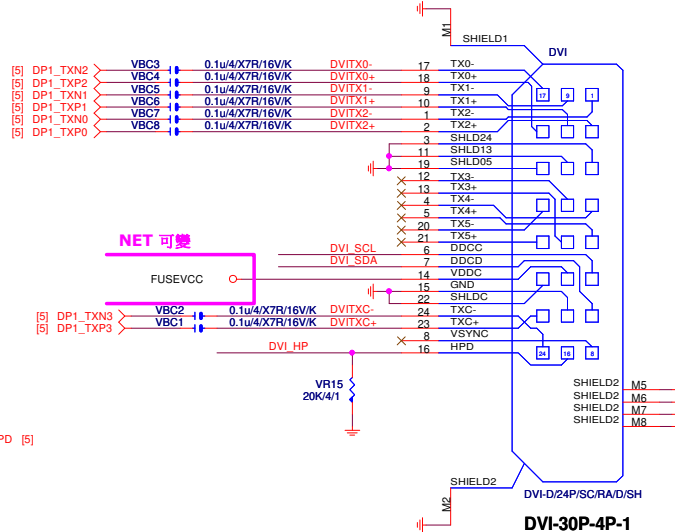
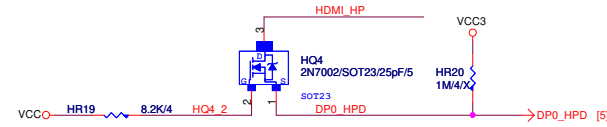
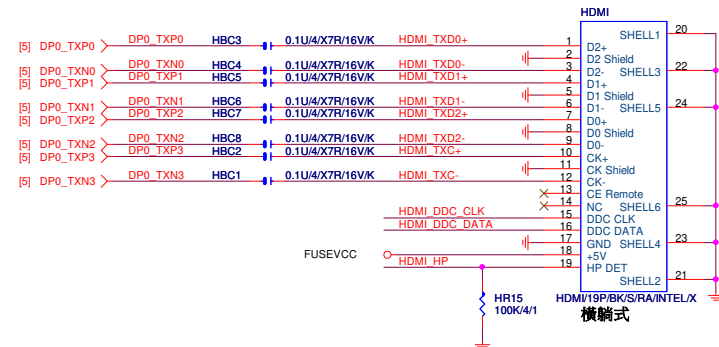


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## M.2 SOCKET

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NET 可變

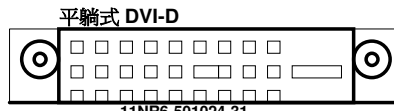
6 DVI\_SCL

5

4 DVI\_SDA

FUSEVCC

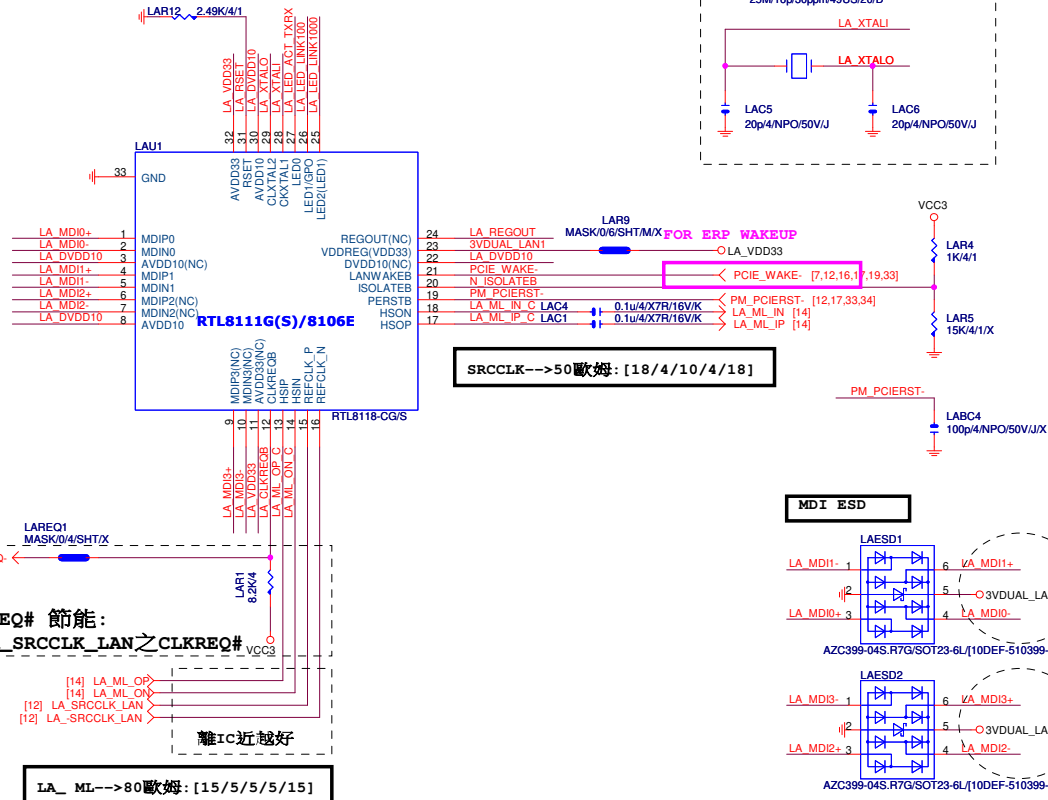
AOZ8902CIL/SOT23-6



Title			
<b>KB_USB_DEC PWR</b>			
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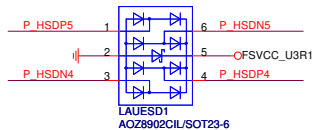


LAN:RTL8111G	R2.03
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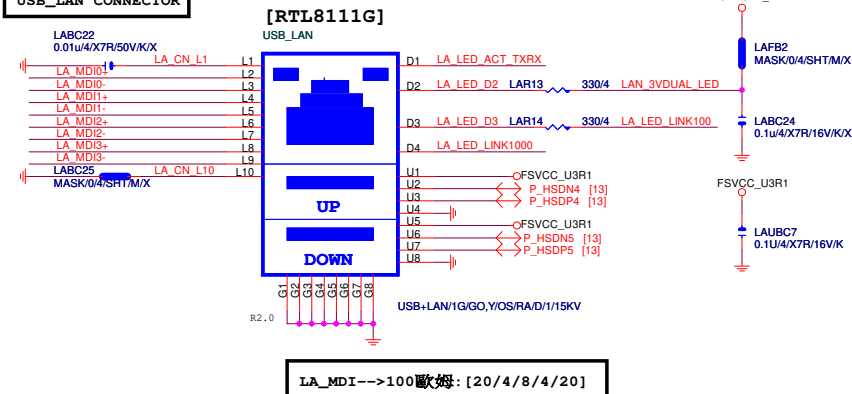


USB_LAN CONNECTOR	R2.03
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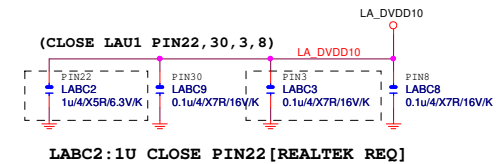
## RMA ESD PROTECT



**USB\_LAN CONNECTOR**

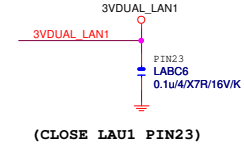


## LAN POWER

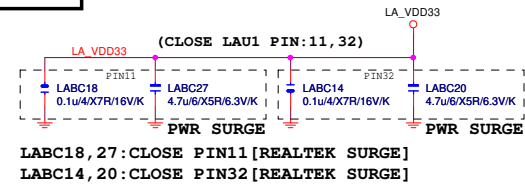


## LAN POWER

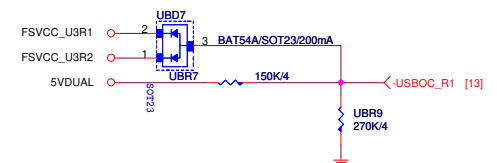
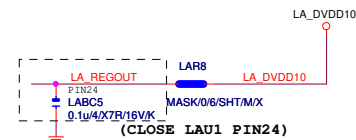
note: lan power連接及電流



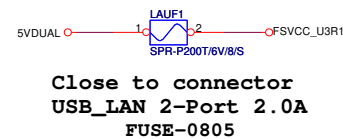
## LAN POWER



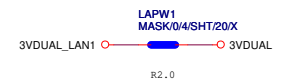
## LAN POWER



## USB POWER



## LAN POWER

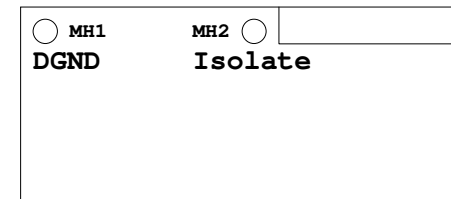
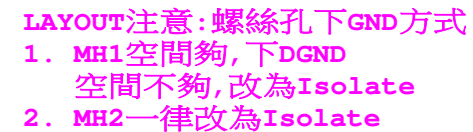


EMI

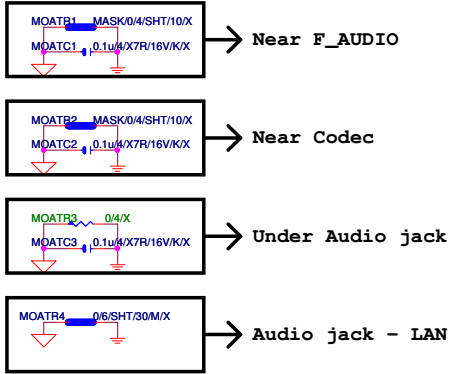
LAN AGND change GND  
Remove Short Pad

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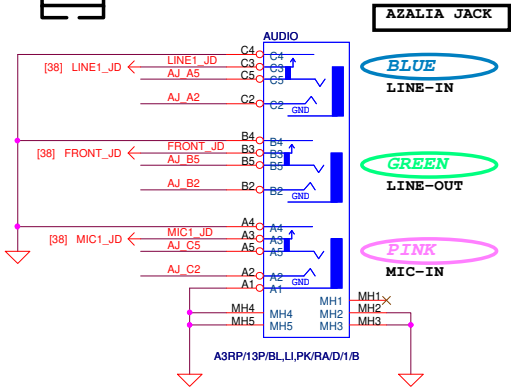
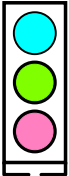




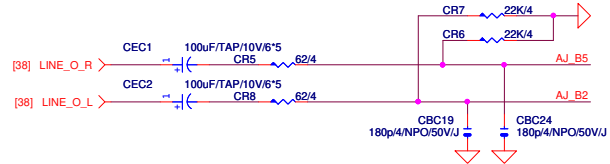


\*量産前, 0ohm改short pad

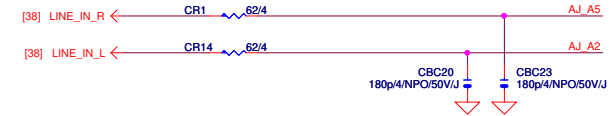
AZALIA JACK



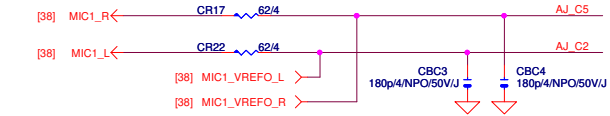
LINE-OUT



LINE-IN



MIC-IN

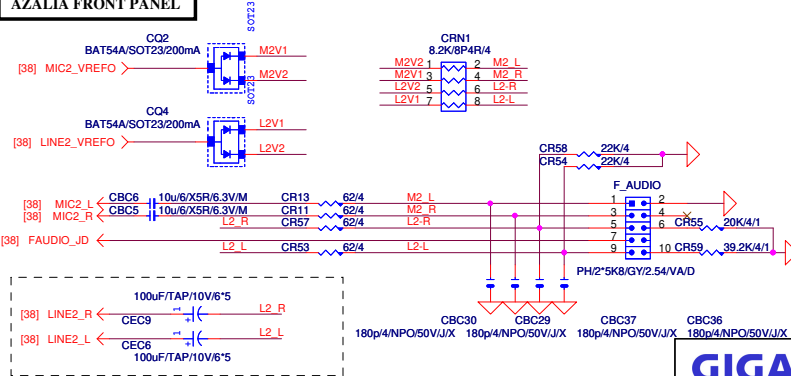


SURROUND

CEN/LFE

SURR BACK

AZALIA FRONT PANEL

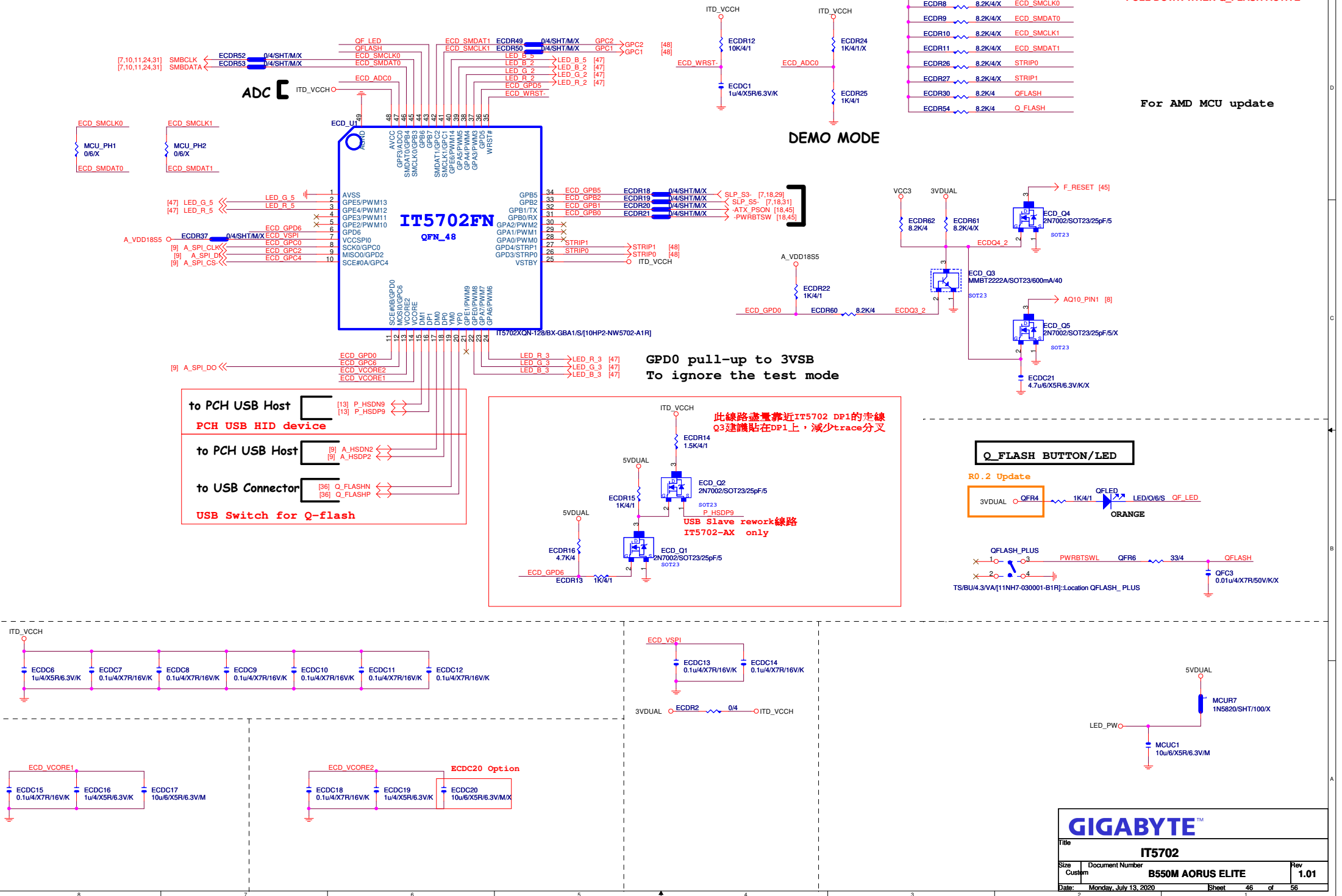


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AUDIO JACK		
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ECD\_U1 請放在PCH到BIOS路徑上. 避免線過長



ECD\_GPD5 ECD\_R4 Q4 Q\_FLASH [29,32]  
PULL DOWN WHEN Q\_FLASH ACTIVE

For AMD MCU update

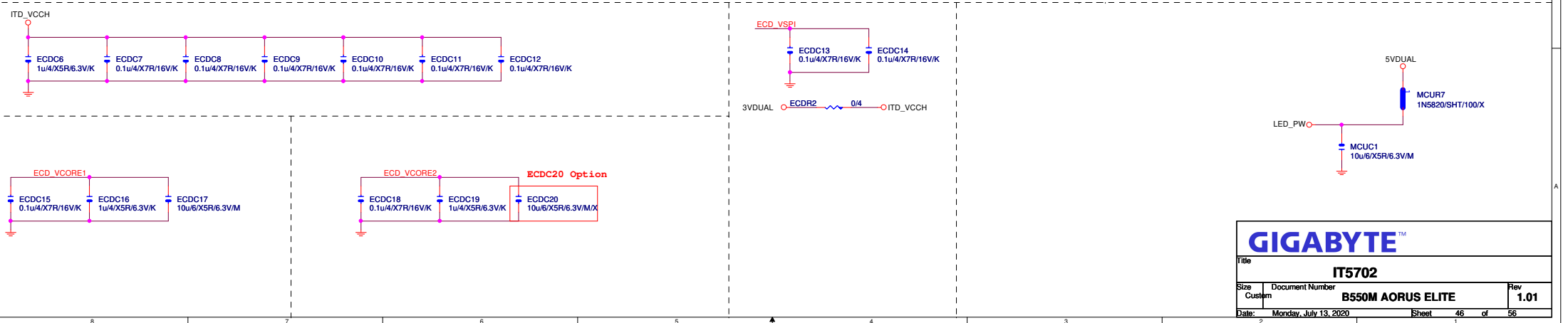
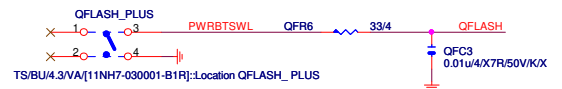
DEMO MODE

GPD0 pull-up to 3VSB  
To ignore the test mode

此線路盡量靠近IT5702 DP1的走線  
Q3建議貼在DP1上, 減少trace分叉

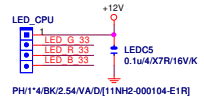
Q\_FLASH BUTTON/LED

R0.2 Update



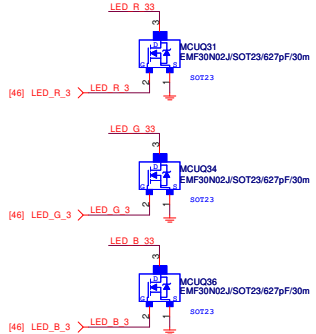
第三區 LED

燈條 LED (LED\_CPU放在CPU附近位置)



Footprint "PH1X4-FAN-AMD-L1"

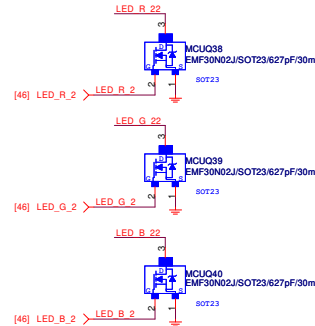
第三區 LED CONTROL



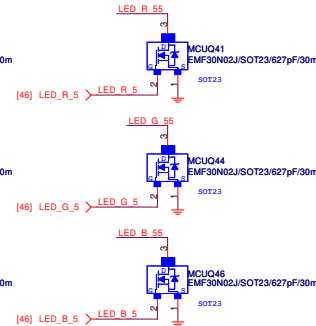
第四區 LED

第五區 LED

第二區 LED CONTROL

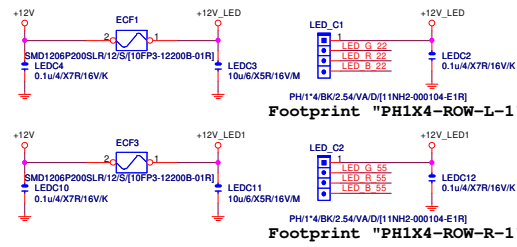


第五區 LED CONTROL



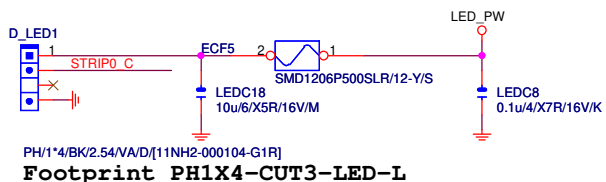
燈條 LED (LED\_C1放在PCB左邊板邊位置)

燈條 LED (LED\_C2放在PCB右邊板邊位置)



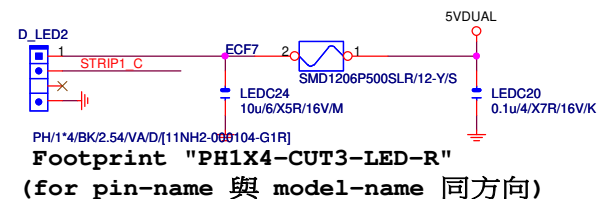
## 第六區 LED (靠近左上板邊位置)

## Digital LED Strip1

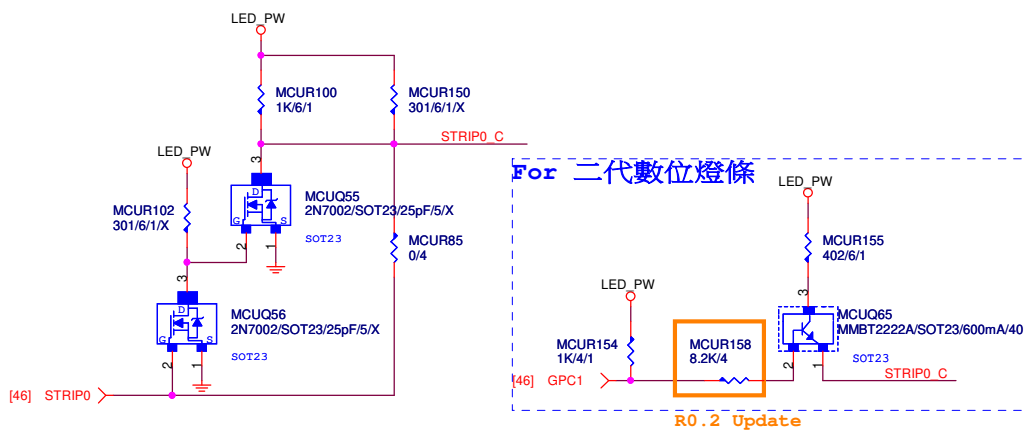


## 第七區 (靠近右下CPU板邊位置)

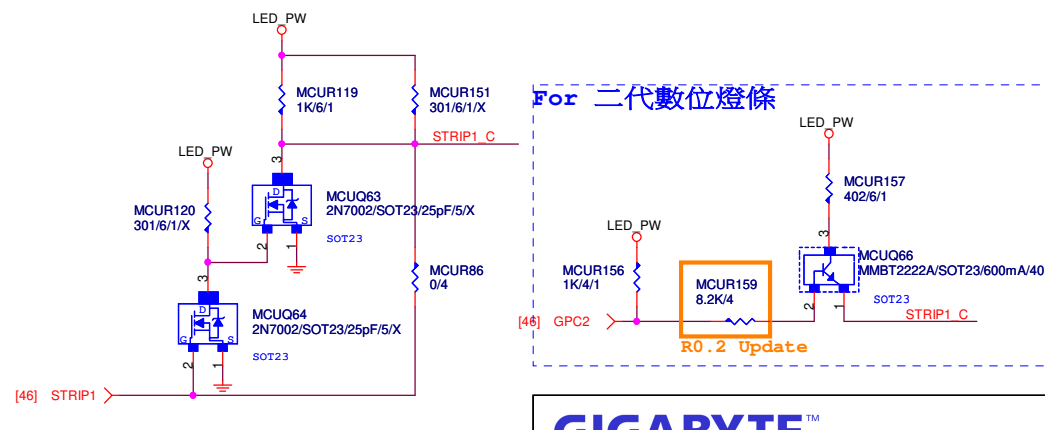
## Digital LED Strip2



## 燈條 Level shift

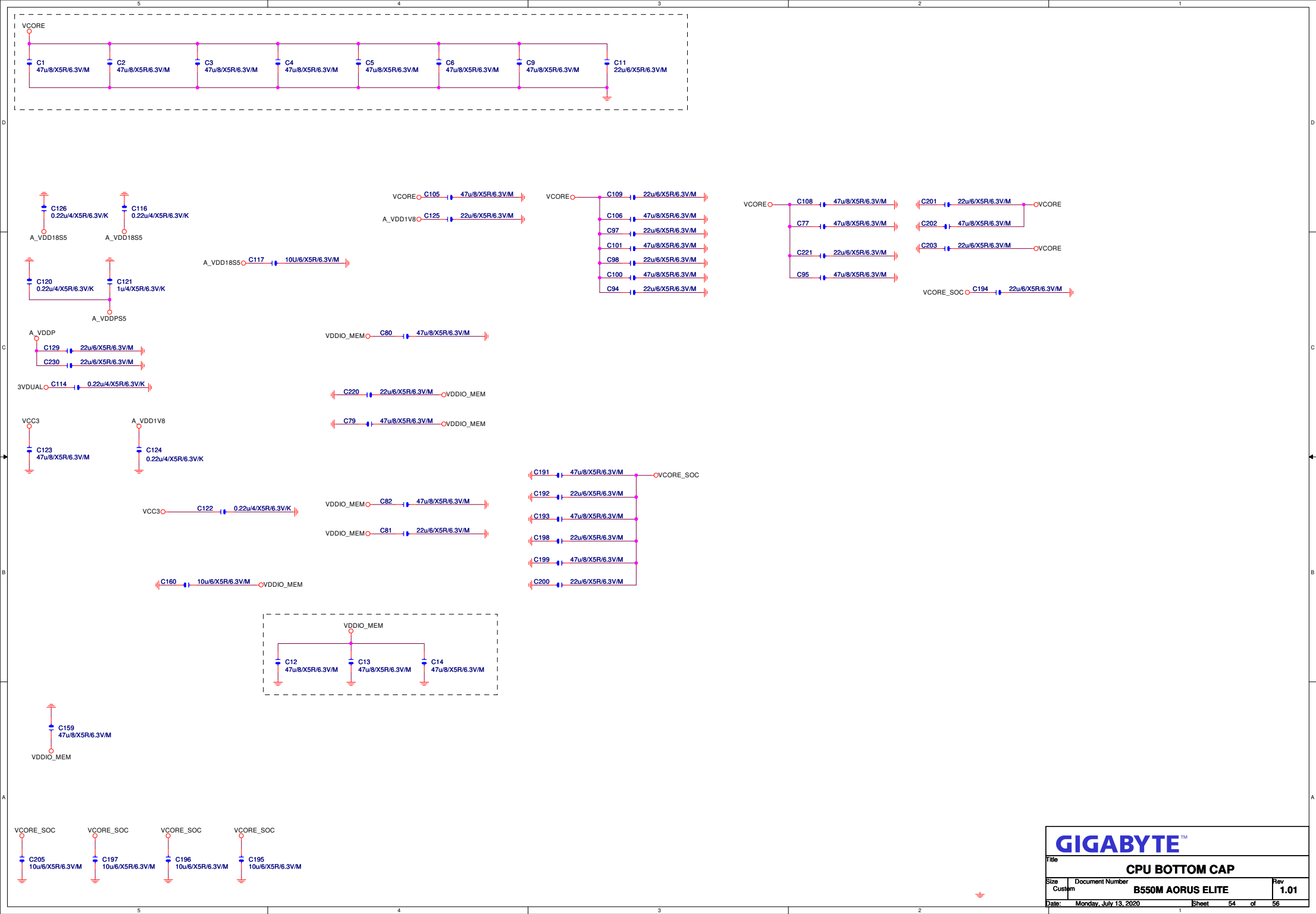


## 燈條 Level shift

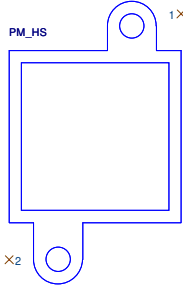
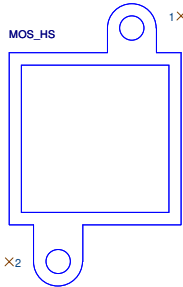
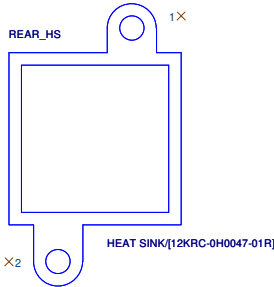
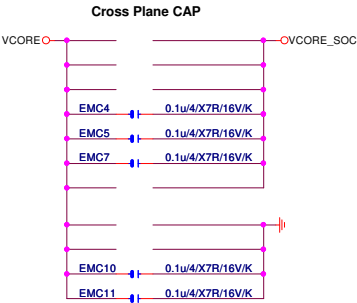
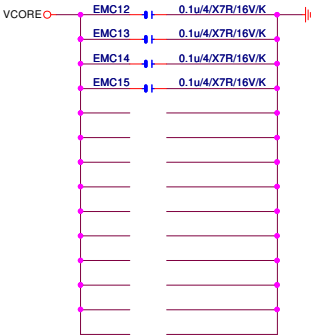
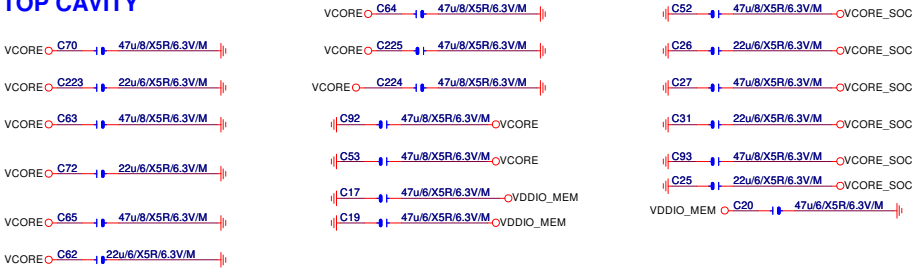


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CPU TOP CAVITY



MOS\_HS

T+R  
Footprint :  
sink\_z490\_ud-t  
HEAT SINK[12SP2-S10840-31R\_12SP2-S10840-32R]

PCH\_HS

Footprint :BGAHSINK\_SB-N  
PM\_HS[12SP2-S03509-51R\_12SP2-S03509-52R]